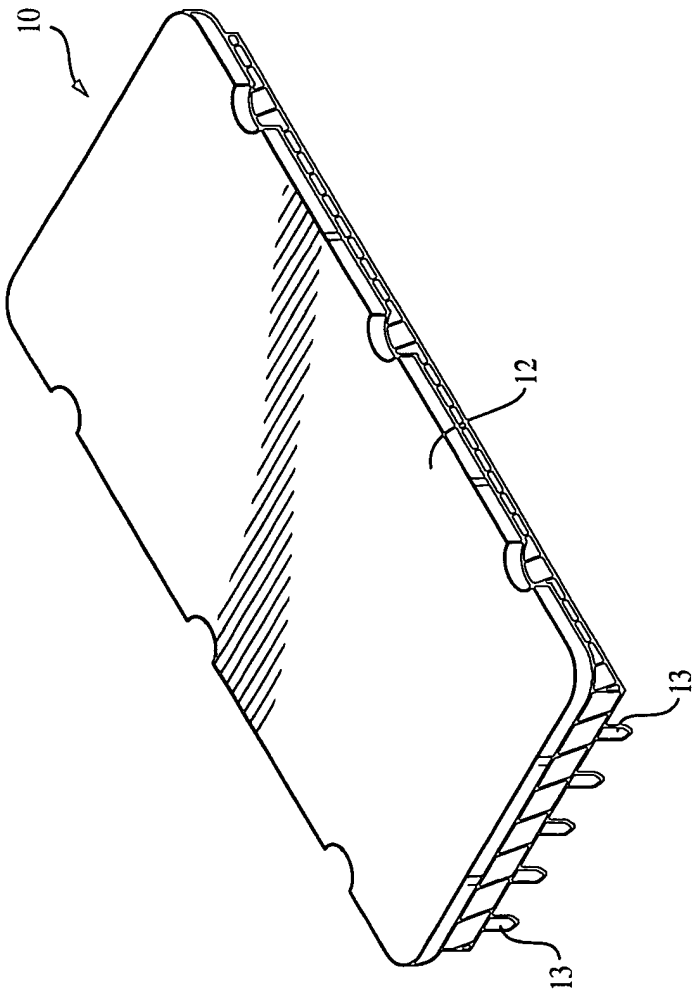


FIG. 1

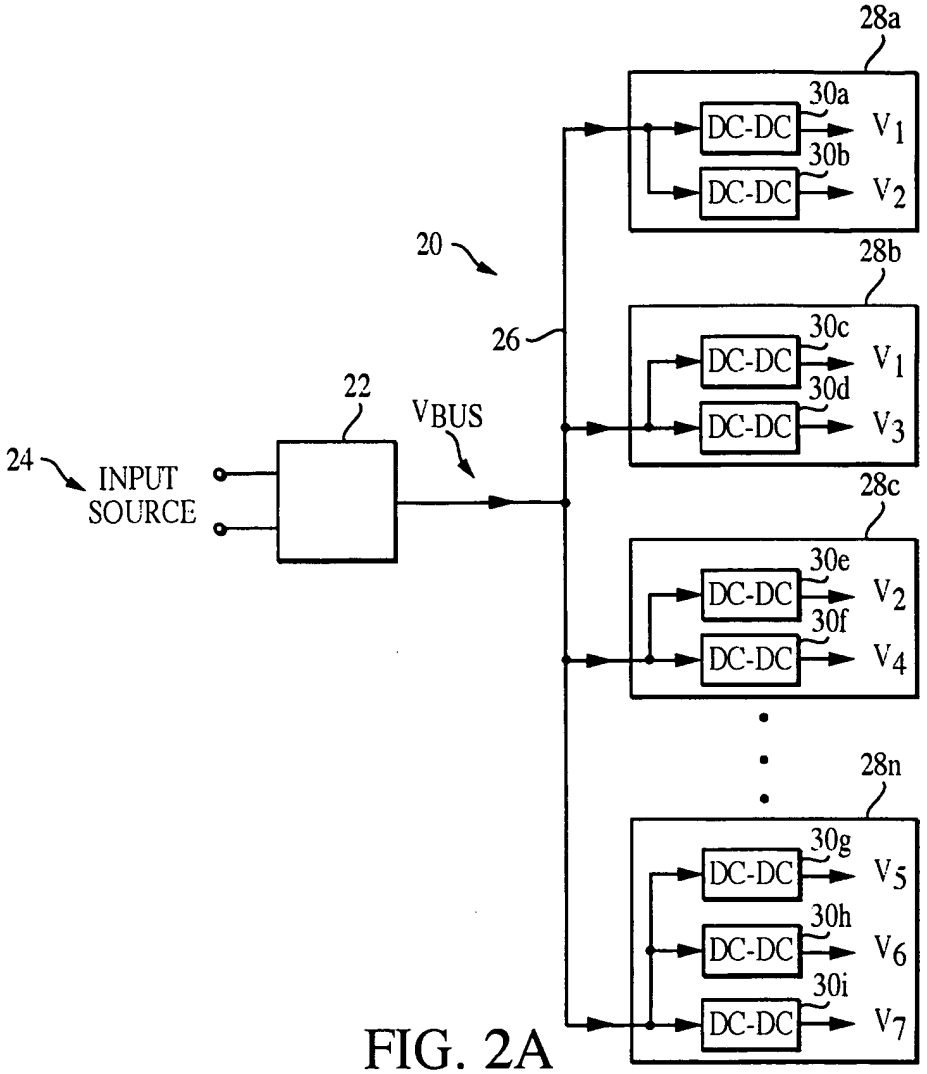

28a
30a
DC-DC
V_1
30b
DC-DC
V_2
20
28b
26
30c
DC-DC
V_1
22
30d
DC-DC
V_3
V_{BUS}
24
INPUT SOURCE
28c
30e
DC-DC
V_2
30f
DC-DC
V_4
28n
30g
DC-DC
V_5
30h
DC-DC
V_6
30i
DC-DC
V_7

FIG. 2A

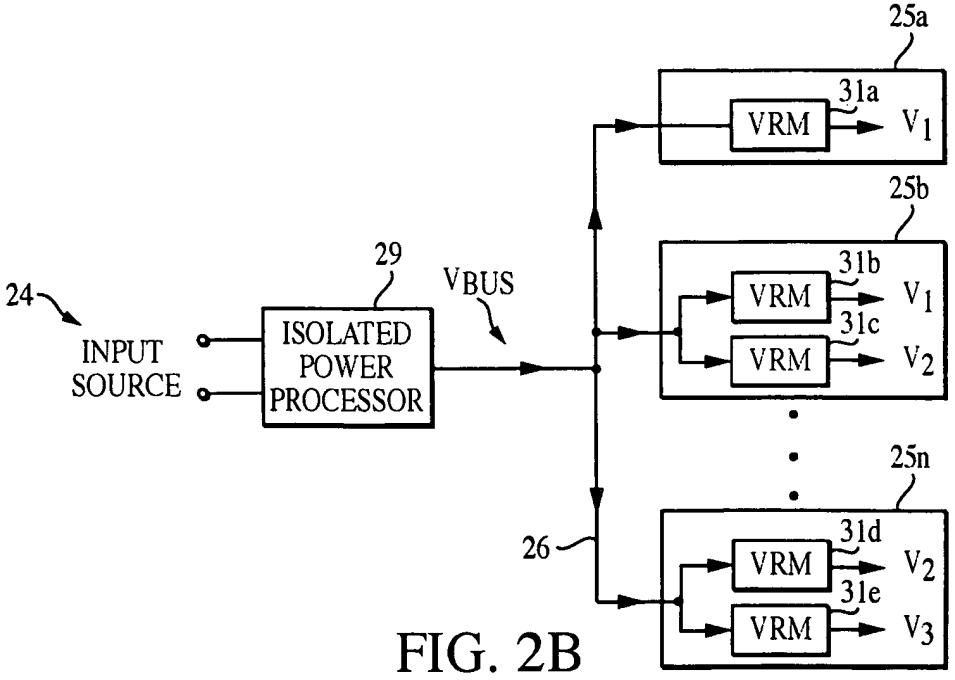

25a
31a
VRM
V_1
25b
29
31b
VRM
V_1
24
V_{BUS}
31c
VRM
V_2
INPUT SOURCE
ISOLATED POWER PROCESSOR
25n
26
31d
VRM
V_2
31e
VRM
V_3

FIG. 2B

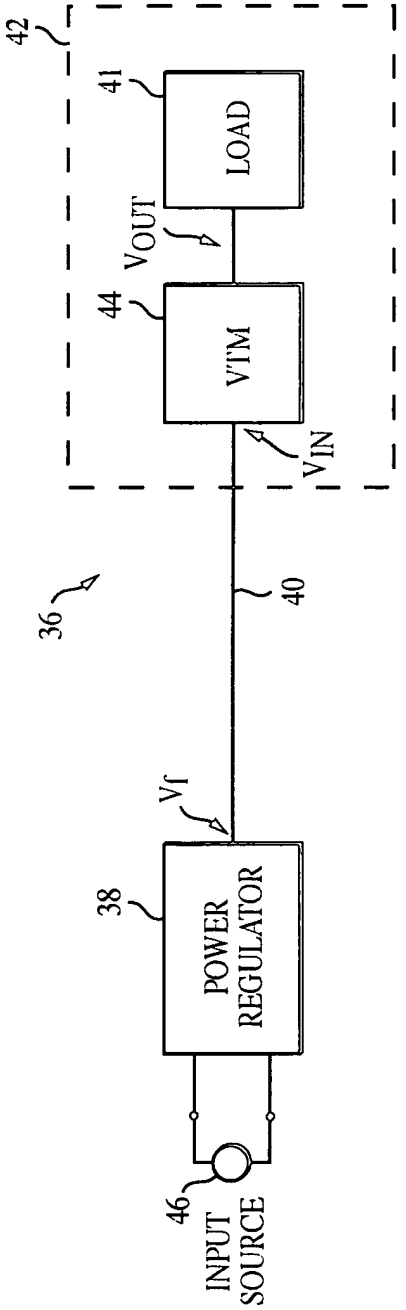

42
41
LOAD
V_{OUT}
44
VTM
V_{IN}
36
40
V_f
38
POWER REGULATOR
46
INPUT SOURCE

FIG. 3A

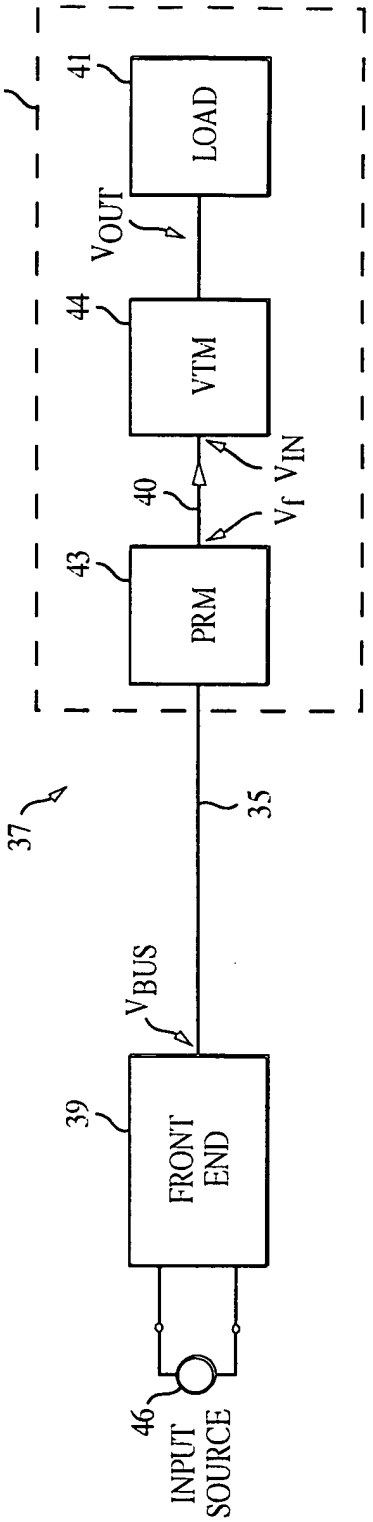

42
41
LOAD
V_{OUT}
44
VTM
V_f V_{IN}
40
43
PRM
37
35
V_{BUS}
39
FRONT END
46
INPUT SOURCE

FIG. 3B

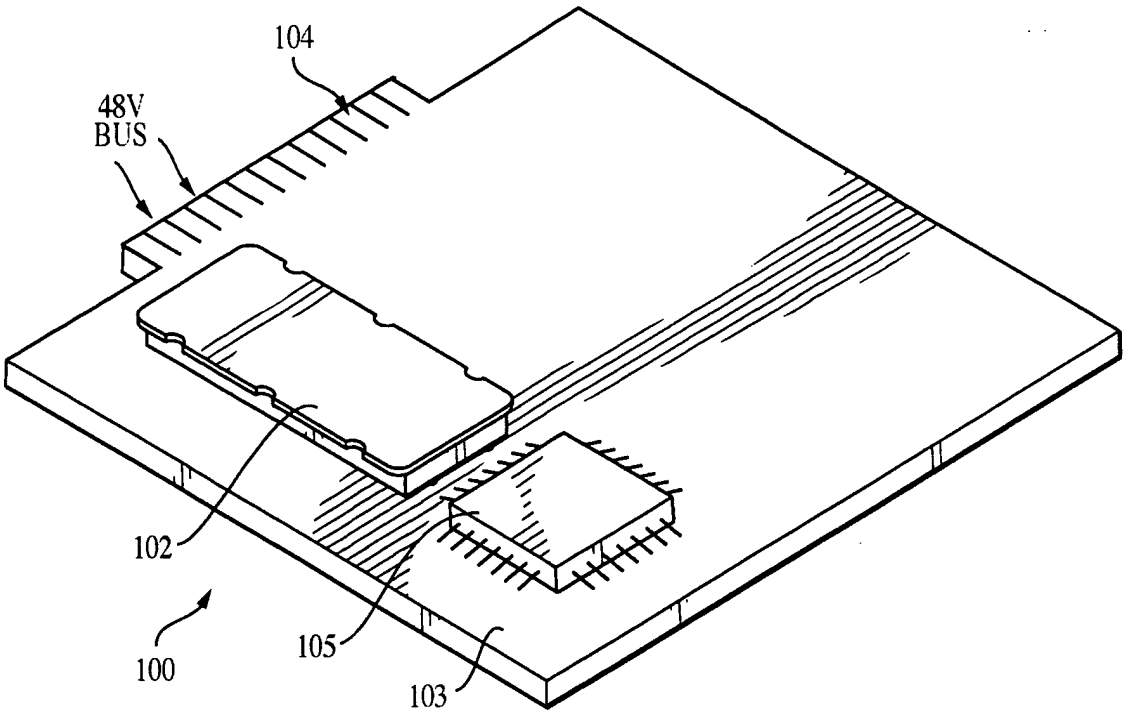


FIG. 4A

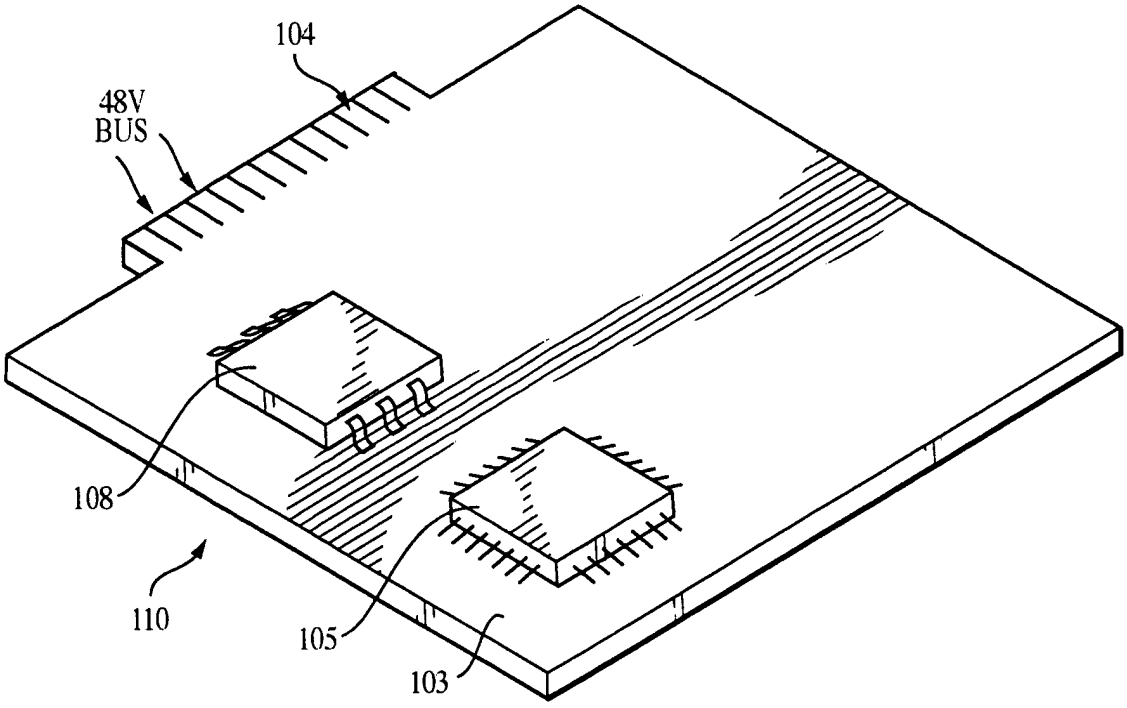


FIG. 4B

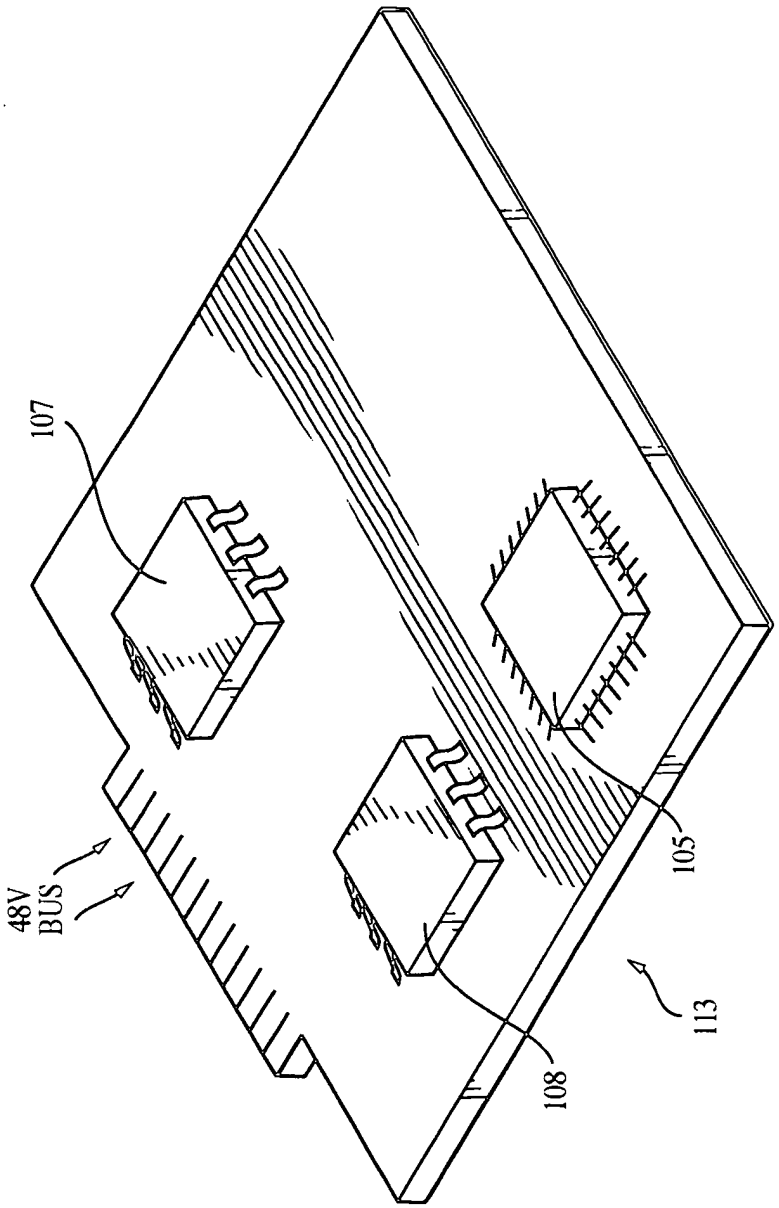


FIG. 4C

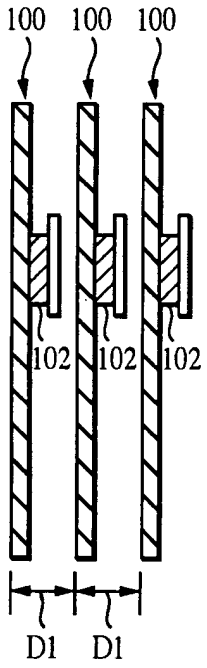

100
100
100
102
102
102
D1
D1

FIG. 5A

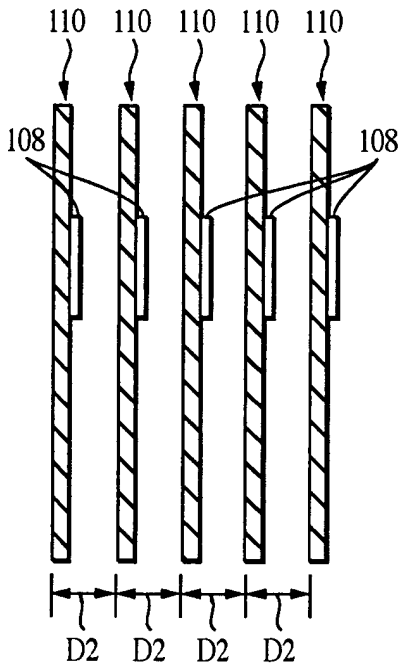

110
110
110
110
110
108
108
D2
D2
D2
D2

FIG. 5B

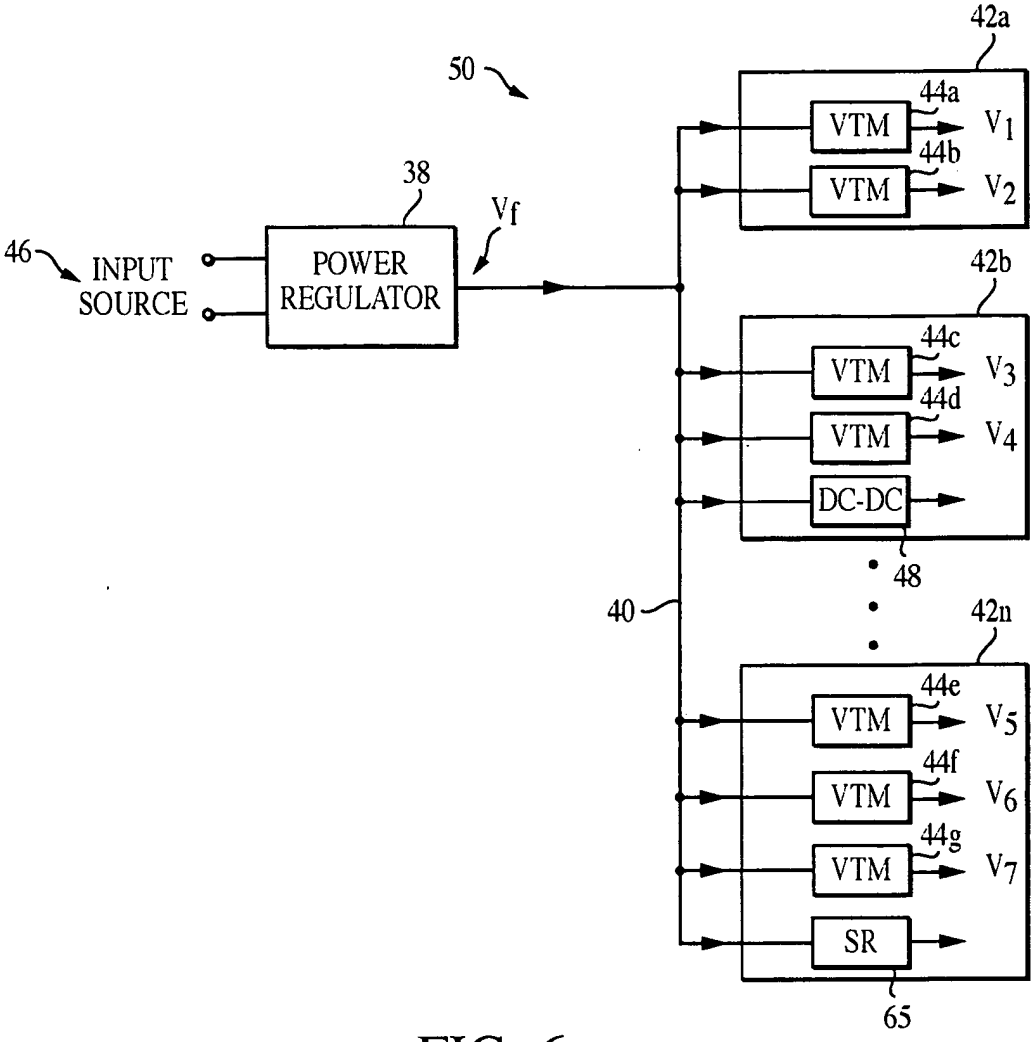

50
38
Vf
46
INPUT SOURCE
POWER REGULATOR
42a
44a
VTM
V1
44b
VTM
V2
42b
44c
VTM
V3
44d
VTM
V4
DC-DC
48
40
42n
44e
VTM
V5
44f
VTM
V6
44g
VTM
V7
SR
65

FIG. 6

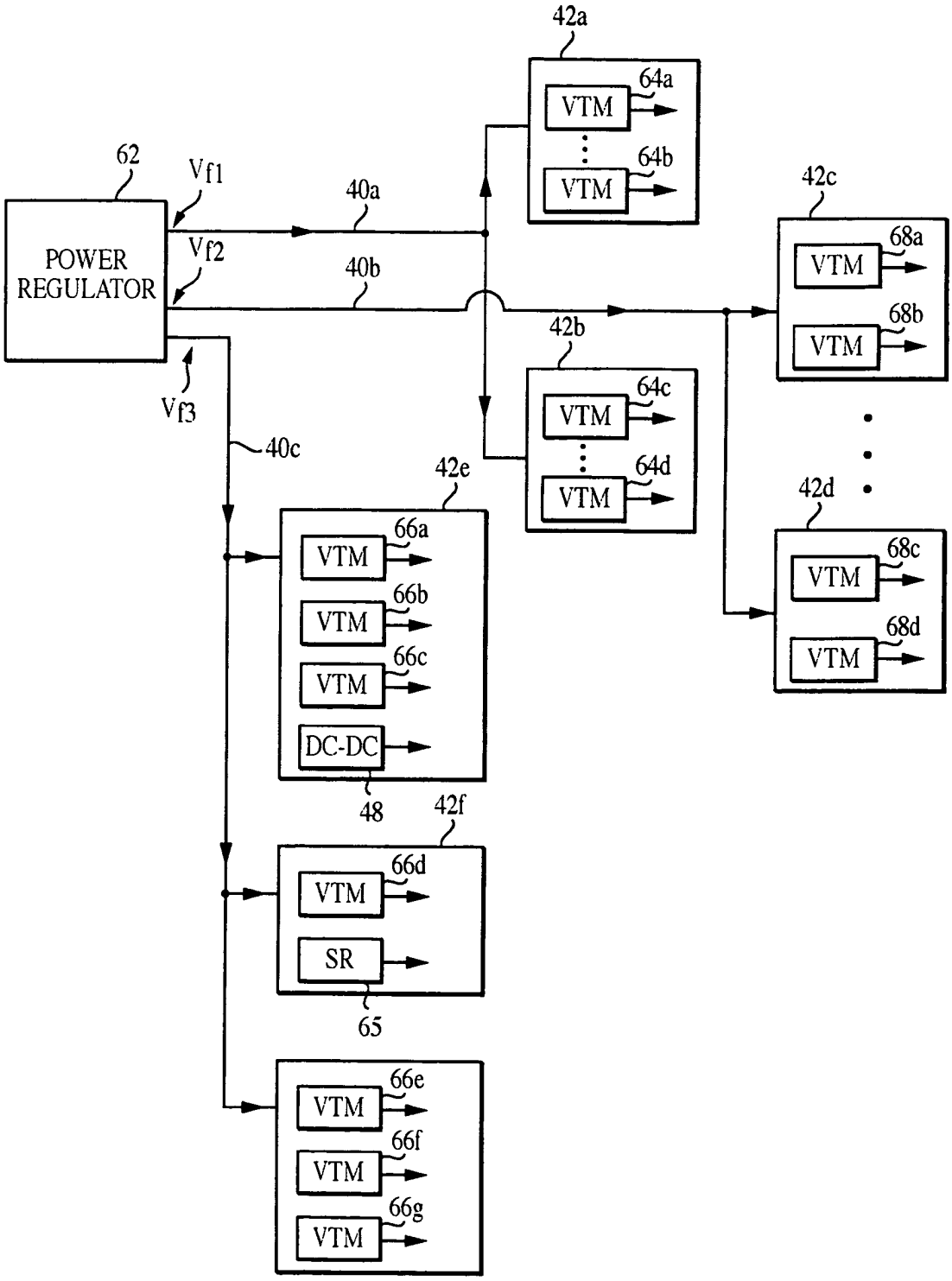

42a
64a
VTM
64b
VTM
62
Vf1
40a
POWER REGULATOR
Vf2
40b
42c
68a
VTM
68b
VTM
42b
64c
VTM
64d
VTM
Vf3
40c
42e
66a
VTM
66b
VTM
66c
VTM
DC-DC
48
42d
68c
VTM
68d
VTM
42f
66d
VTM
SR
65
66e
VTM
66f
VTM
66g
VTM

FIG. 7

FIG. 8A

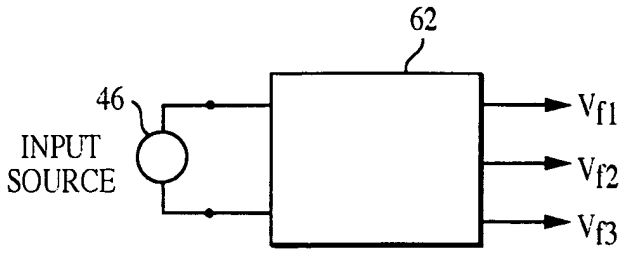


FIG. 8B

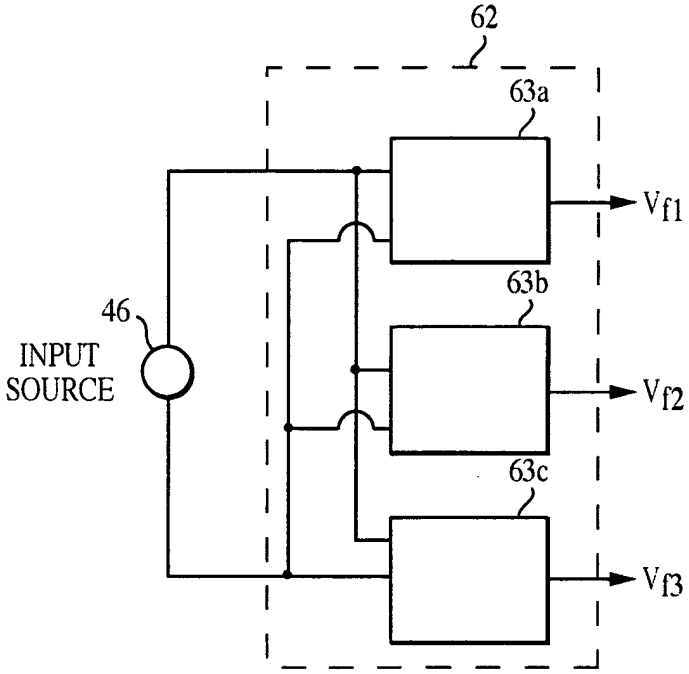
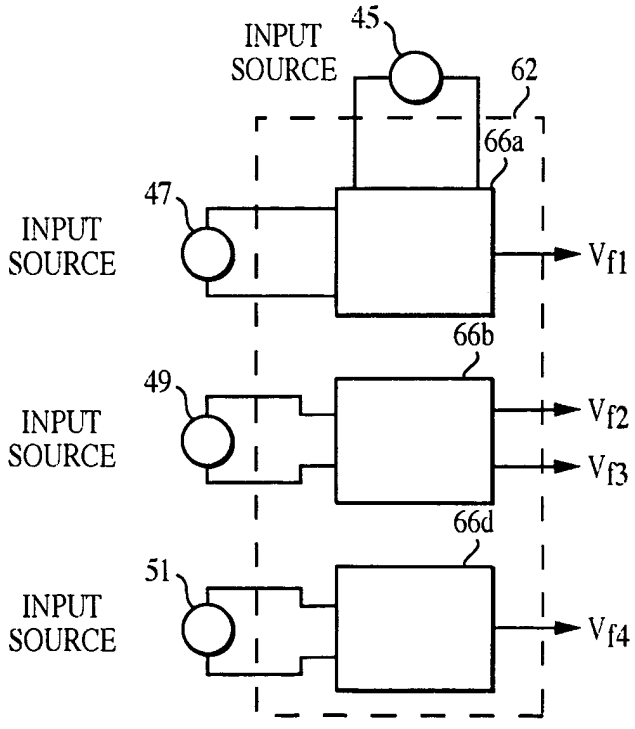


FIG. 8C



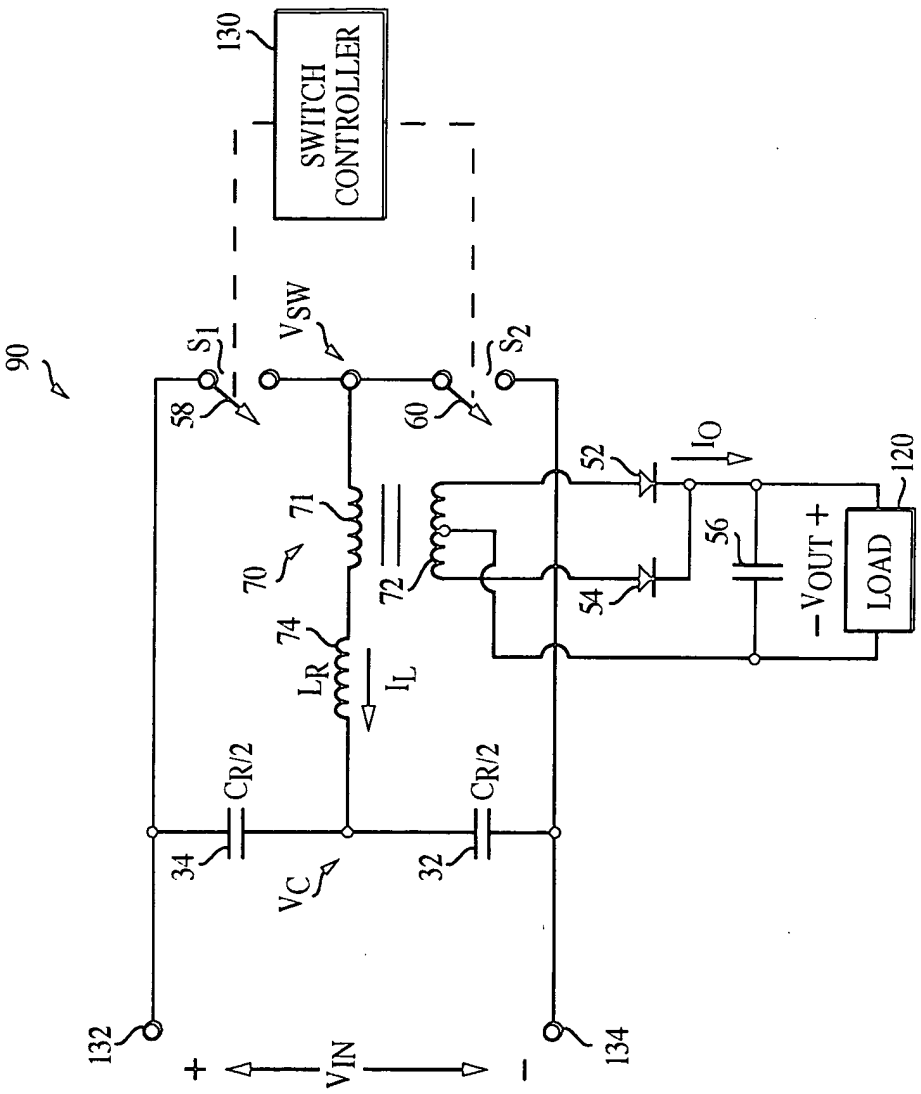

90
130
SWITCH CONTROLLER
S_1
V_{SW}
S_2
58
60
52
I_O
120
71
70
72
54
56
$-V_{OUT}+$
LOAD
74
L_R
I_L
$C_R/2$
$C_R/2$
34
32
V_C
132
134
+
V_{IN}
−

FIG. 9

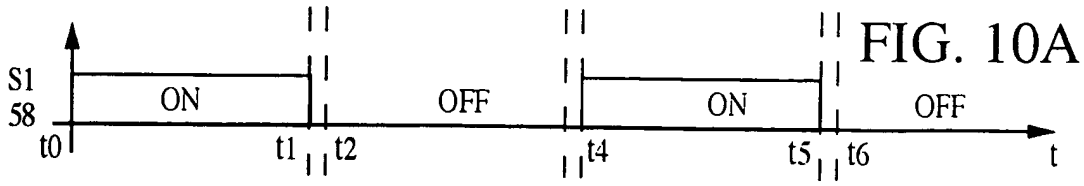


FIG. 10A

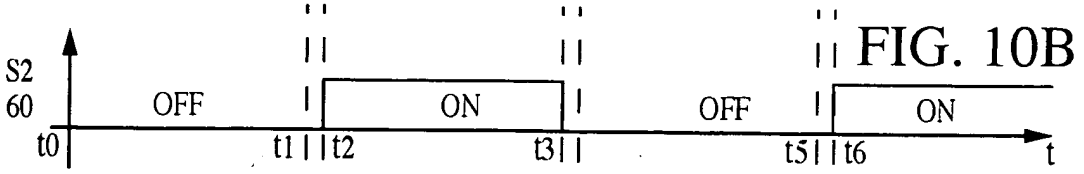


FIG. 10B

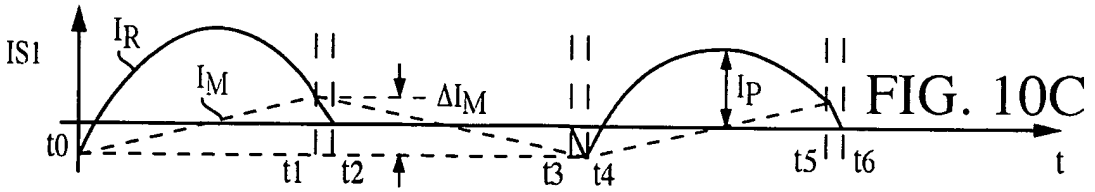


FIG. 10C

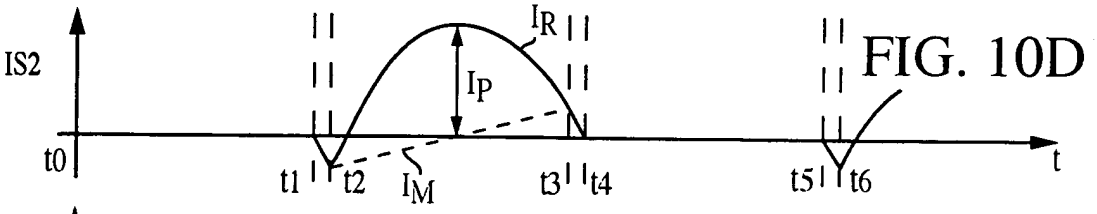


FIG. 10D

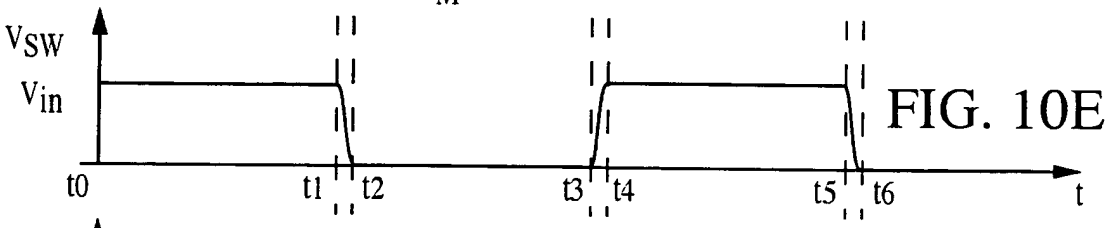


FIG. 10E

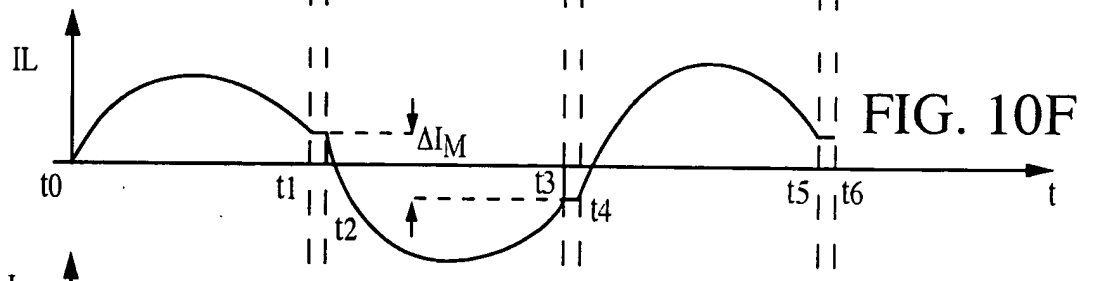


FIG. 10F

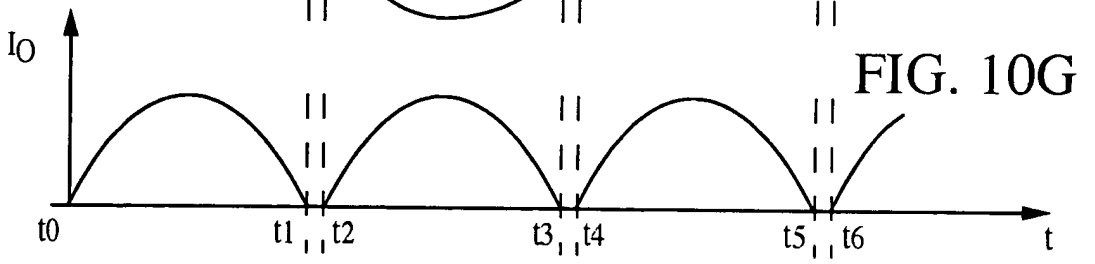


FIG. 10G

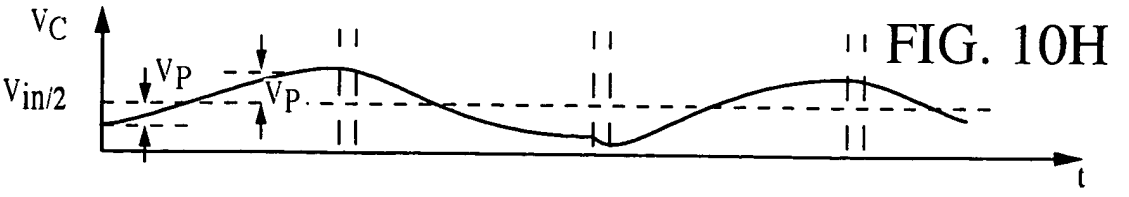


FIG. 10H

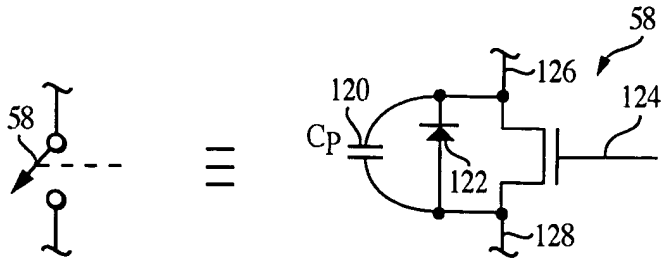


FIG. 11

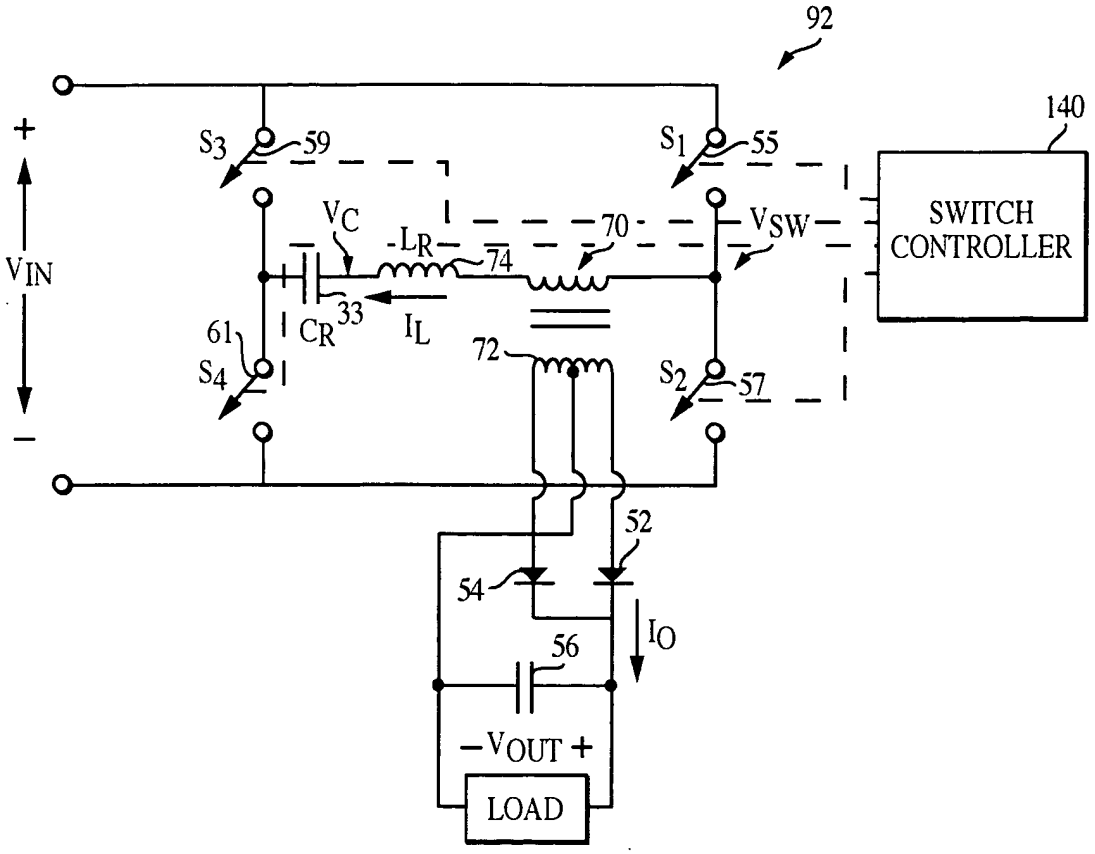

92
140
+
VIN
–
S3
59
S1
55
SWITCH CONTROLLER
VC
LR
70
VSW
74
CR
33
IL
61
S4
72
S2
57
52
54
IO
56
–VOUT+
LOAD

FIG. 12

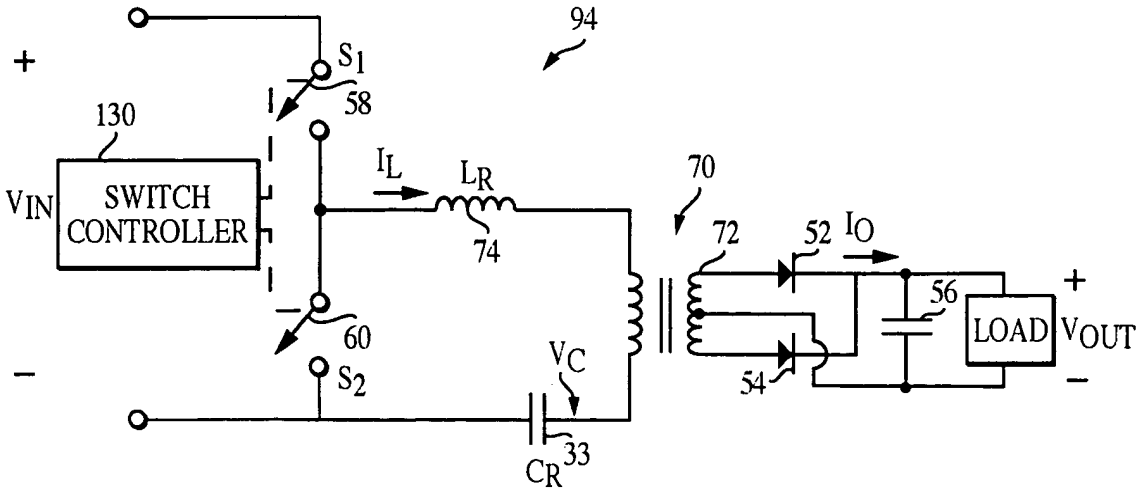

94
+
S1
58
130
VIN
SWITCH CONTROLLER
IL
LR
70
74
72
52
IO
56
+
LOAD
VOUT
–
60
S2
VC
54
CR
33

FIG. 13

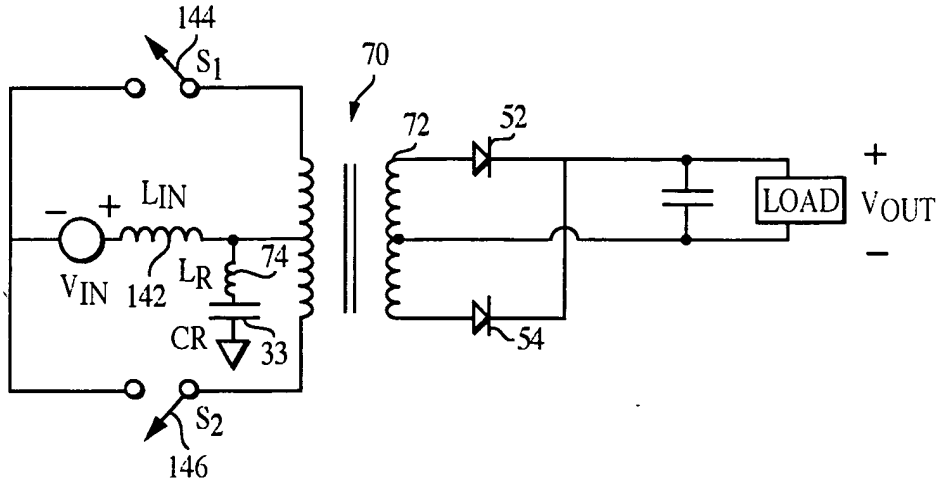


FIG. 14

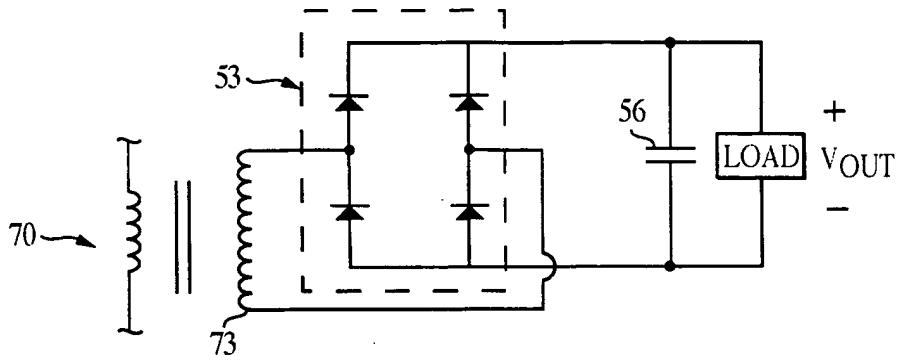


FIG. 15A

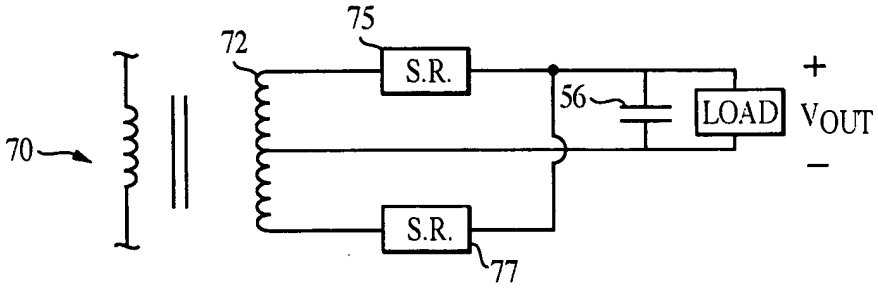


FIG. 15B

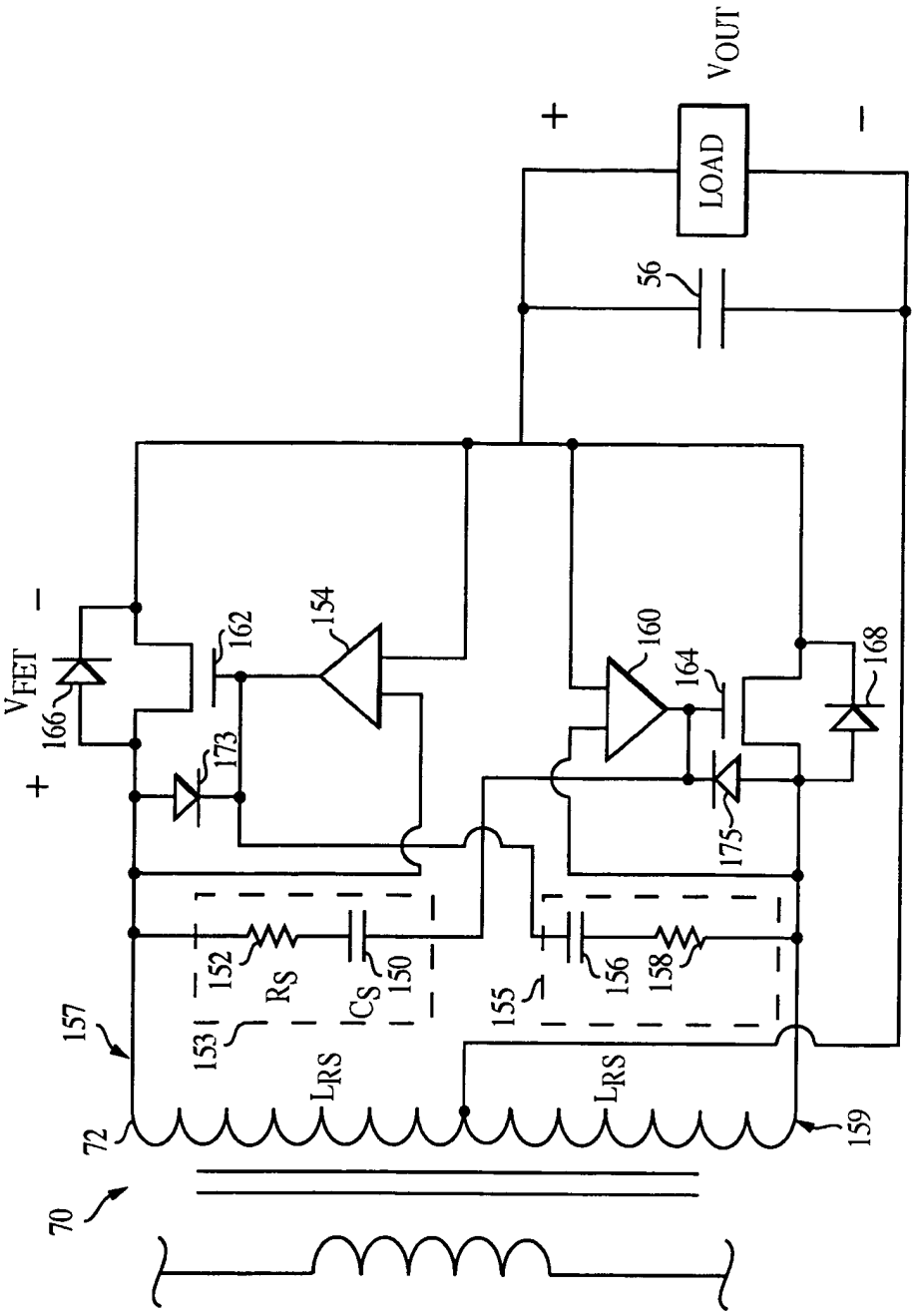

VOUT
+
LOAD
−
56
VFET
166
162
154
160
164
168
173
175
152
RS
CS
150
155
156
158
153
157
LRS
LRS
72
159
70

FIG. 15C

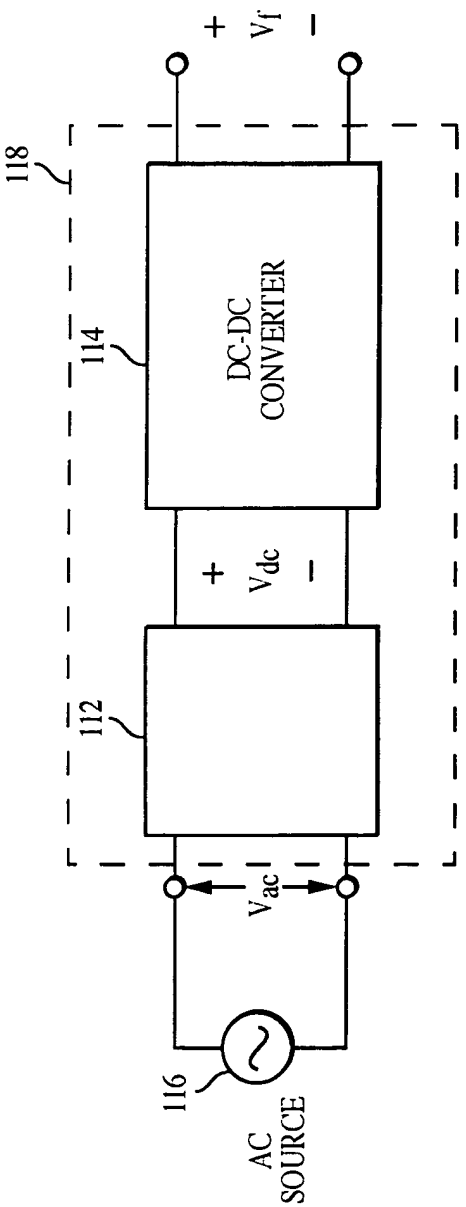

+ V_f −
118
114
DC-DC
CONVERTER
+ V_{dc} −
112
V_{ac}
116
AC
SOURCE

FIG. 16

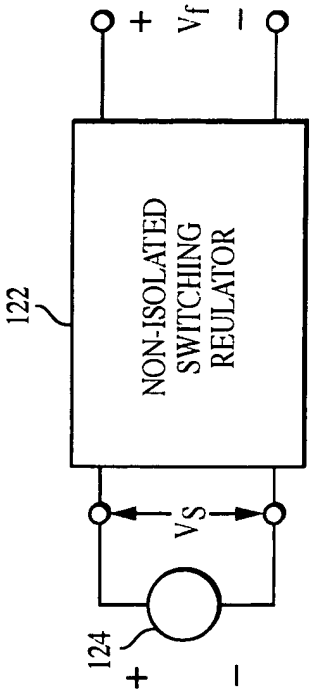

+ V_f −
122
NON-ISOLATED
SWITCHING
REULATOR
V_S
124
+
−

FIG. 17

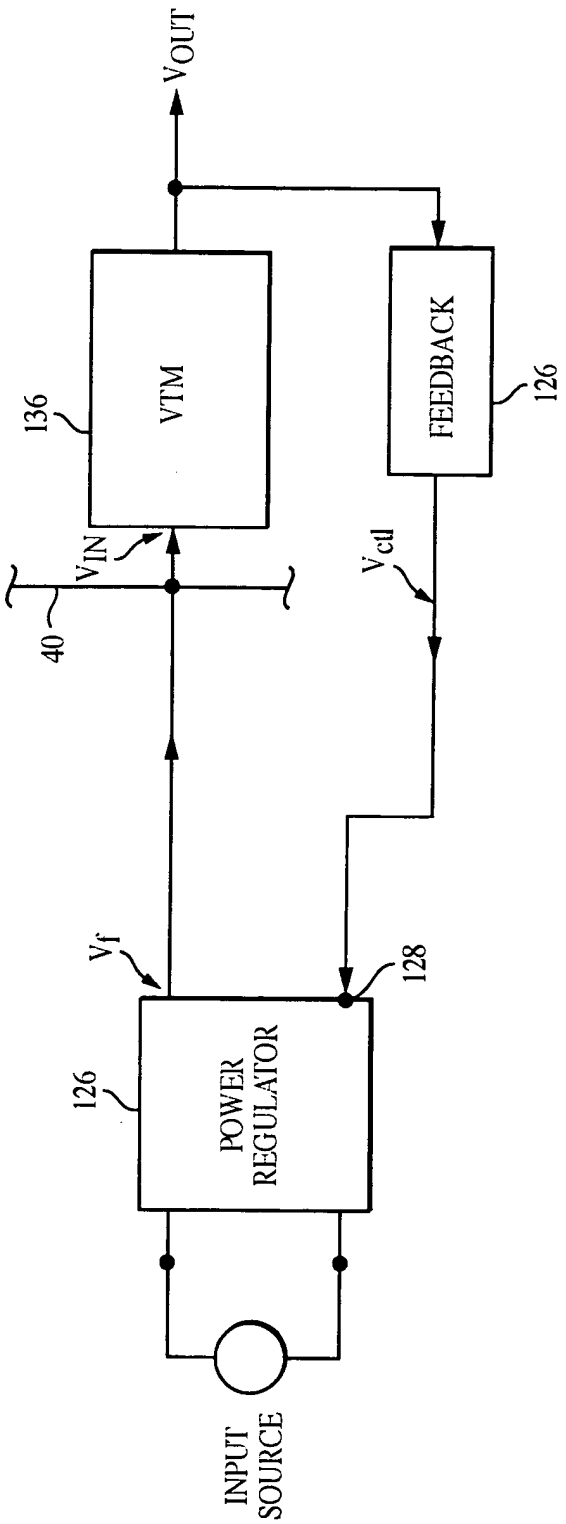

VOUT
VTM
136
FEEDBACK
126
VIN
40
Vctl
Vf
128
POWER
REGULATOR
126
INPUT
SOURCE

FIG. 18

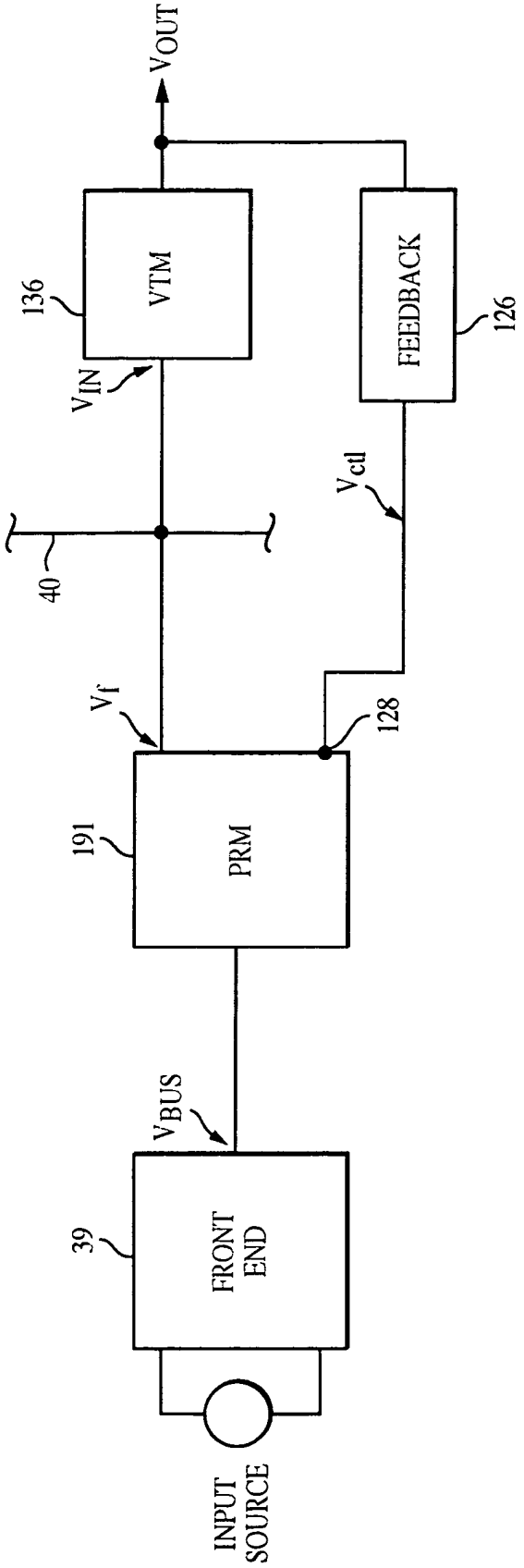

V_{OUT}
VTM
136
FEEDBACK
126
V_{IN}
V_{ctl}
40
V_f
128
PRM
191
V_{BUS}
FRONT END
39
INPUT SOURCE

FIG. 19

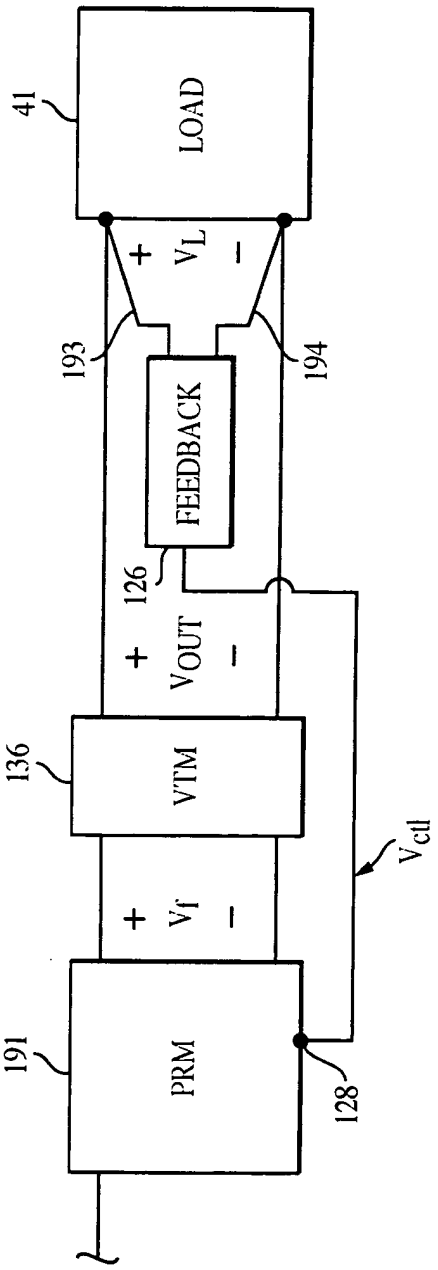

41
LOAD
+ V_L −
193
194
FEEDBACK
126
+ V_{OUT} −
136
VTM
+ V_f −
V_{ctl}
191
PRM
128

FIG. 20

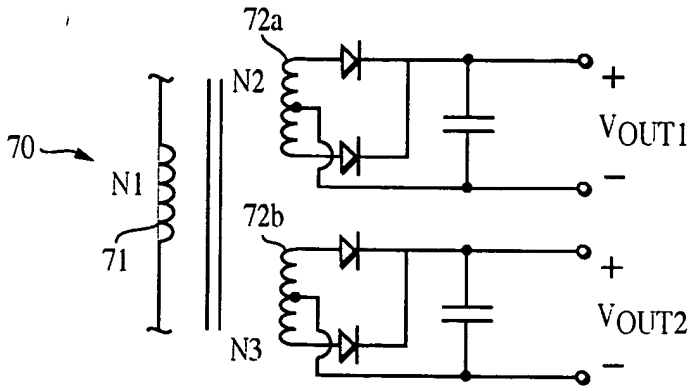


FIG. 21

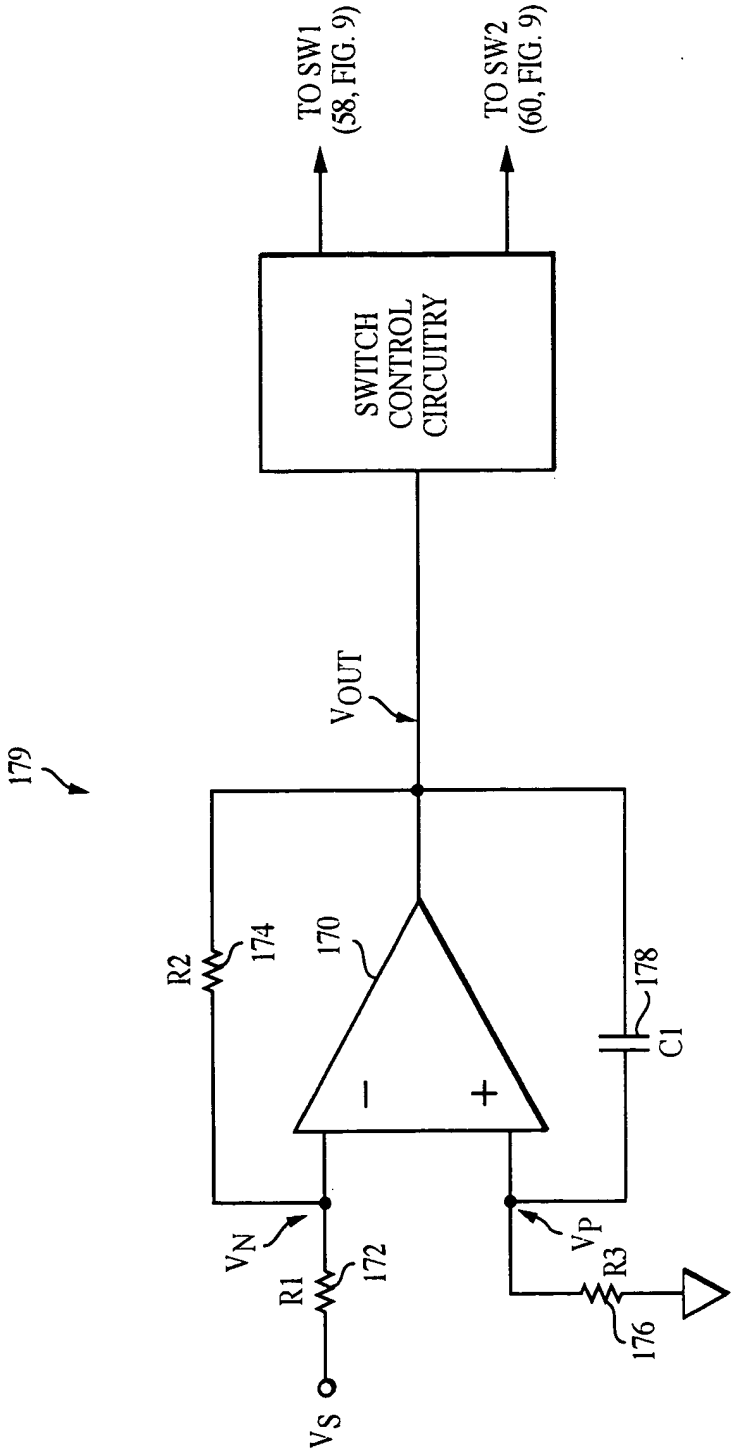

TO SW1 (58, FIG. 9)
TO SW2 (60, FIG. 9)
SWITCH CONTROL CIRCUITRY
VOUT
179
R2
174
170
178
C1
VN
VP
R1
172
R3
176
VS

FIG. 22

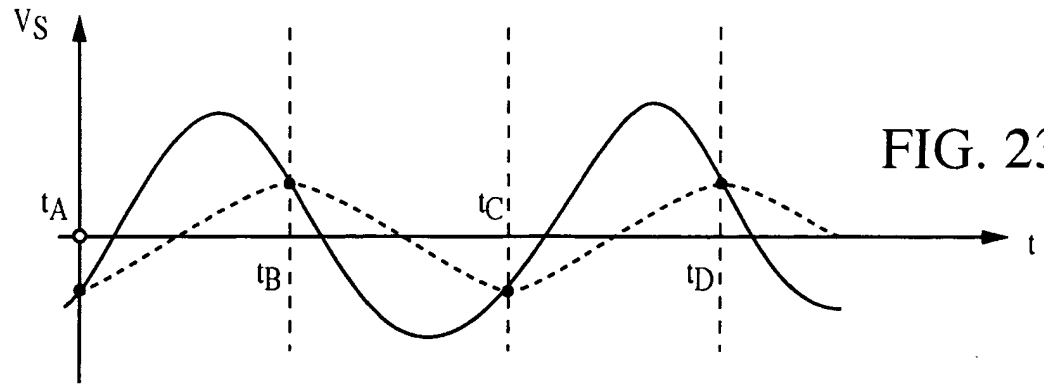


FIG. 23A

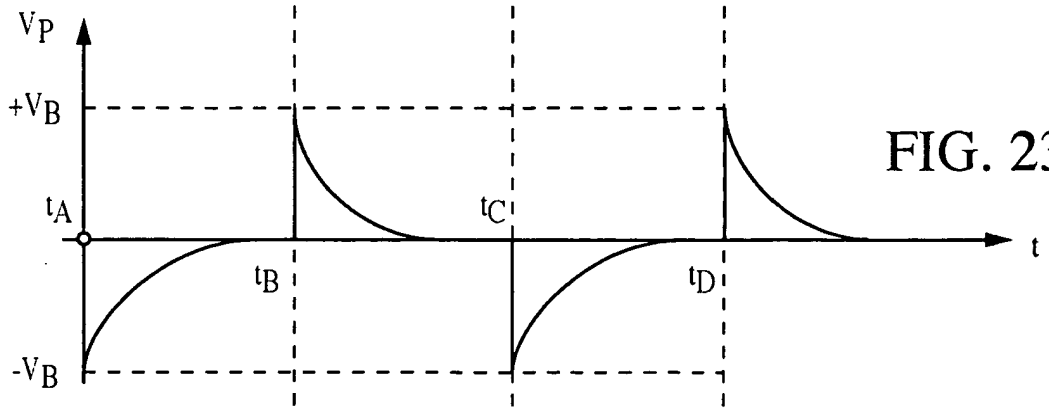


FIG. 23B

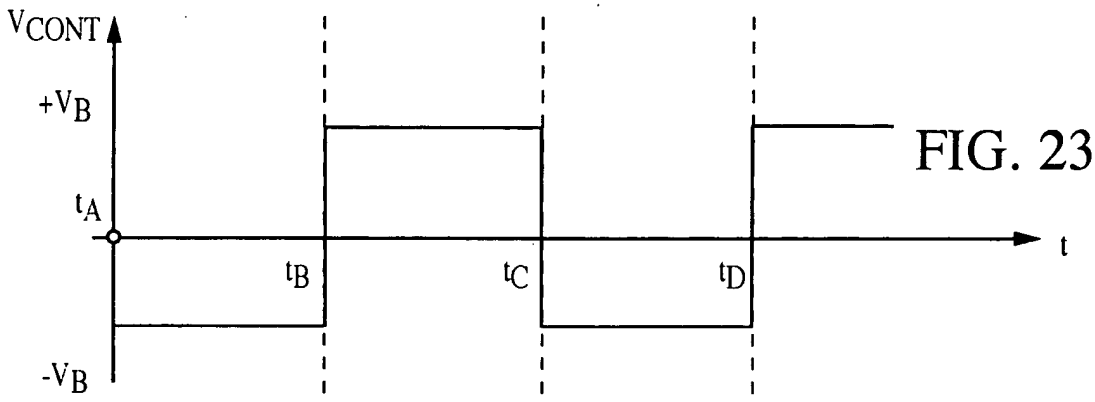


FIG. 23C

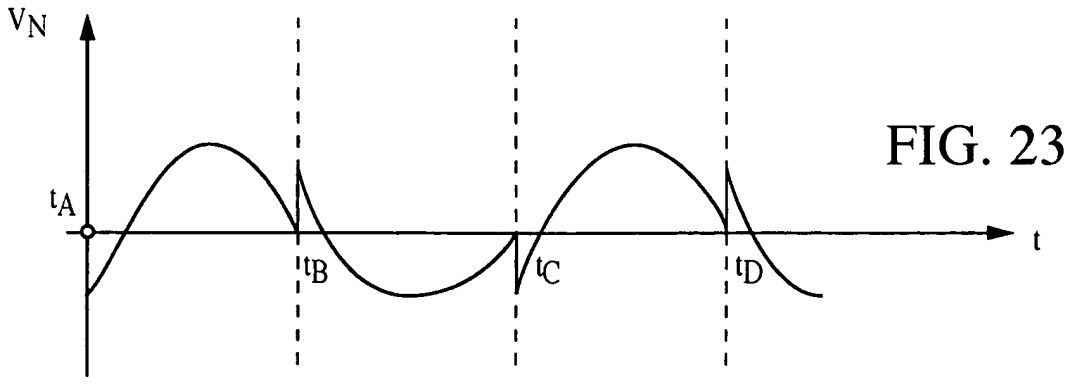


FIG. 23D

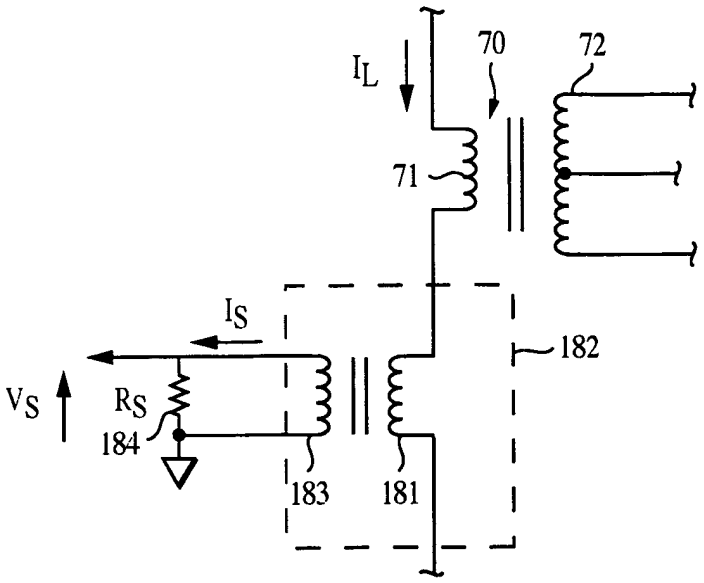


FIG. 24

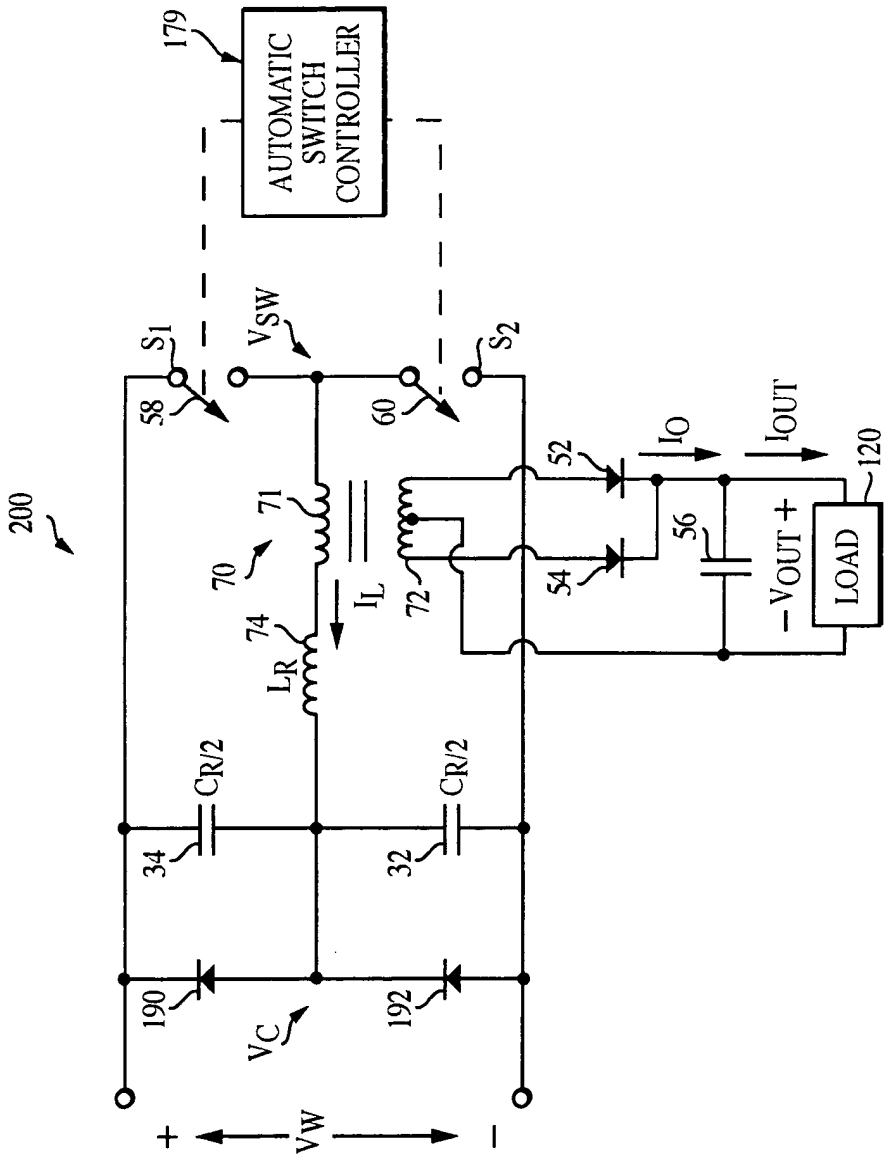

200
179
AUTOMATIC SWITCH CONTROLLER
S1
VSW
S2
58
60
52
IO
IOUT
120
71
70
IL
72
54
56
74
LR
−VOUT +
LOAD
CR/2
CR/2
34
32
190
192
VC
+
VW
−

FIG. 25

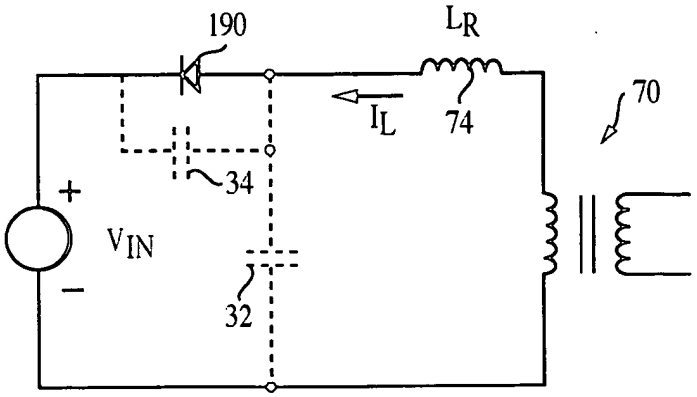


FIG. 26

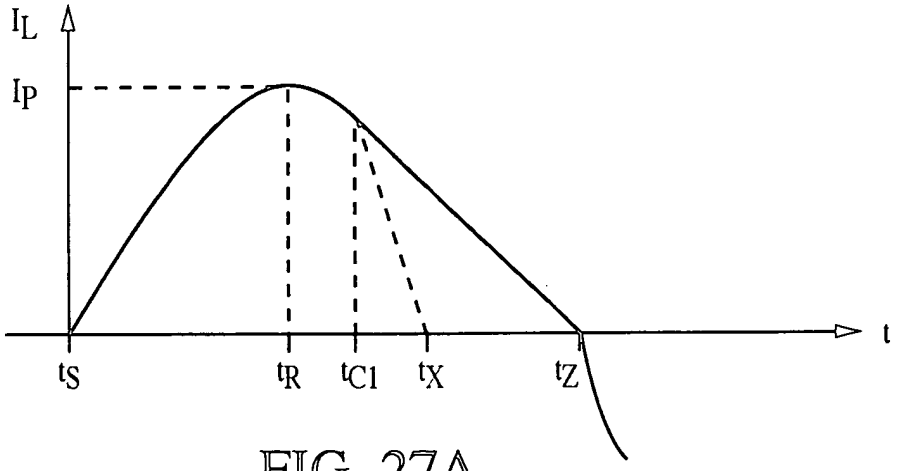


FIG. 27A

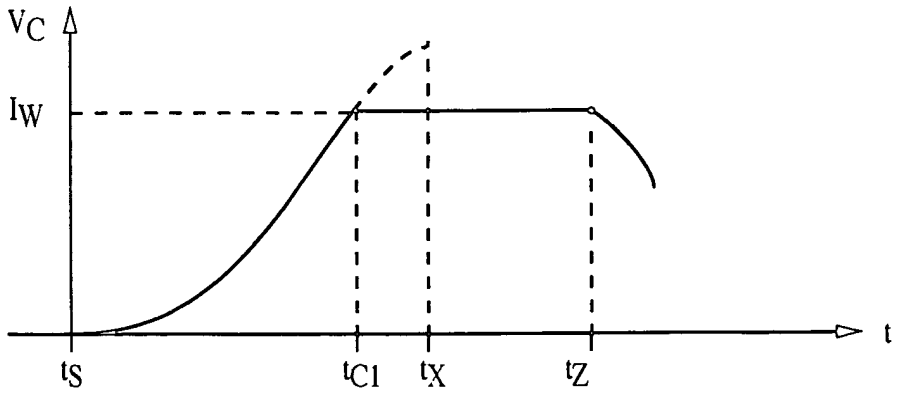


FIG. 27B

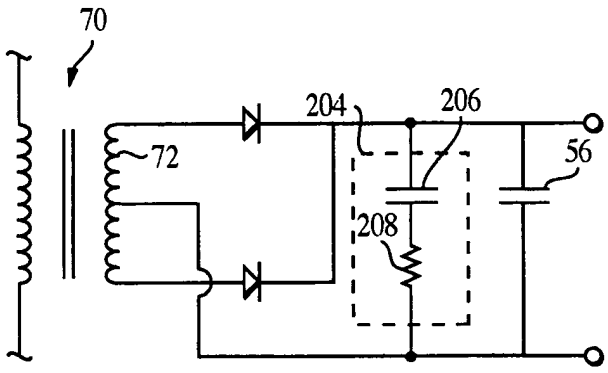


FIG. 28

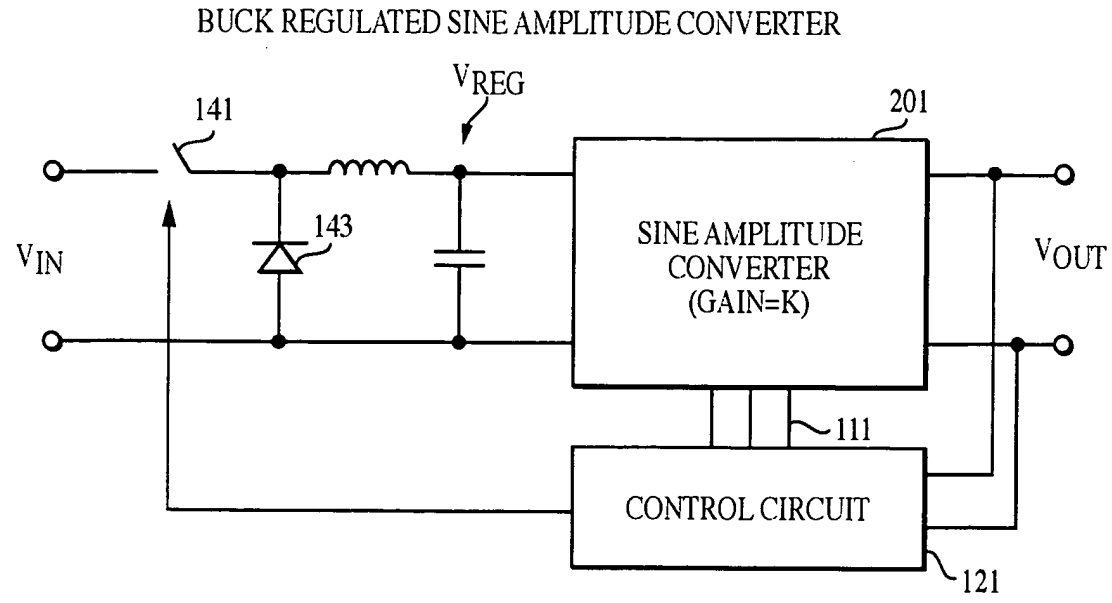


FIG. 29A

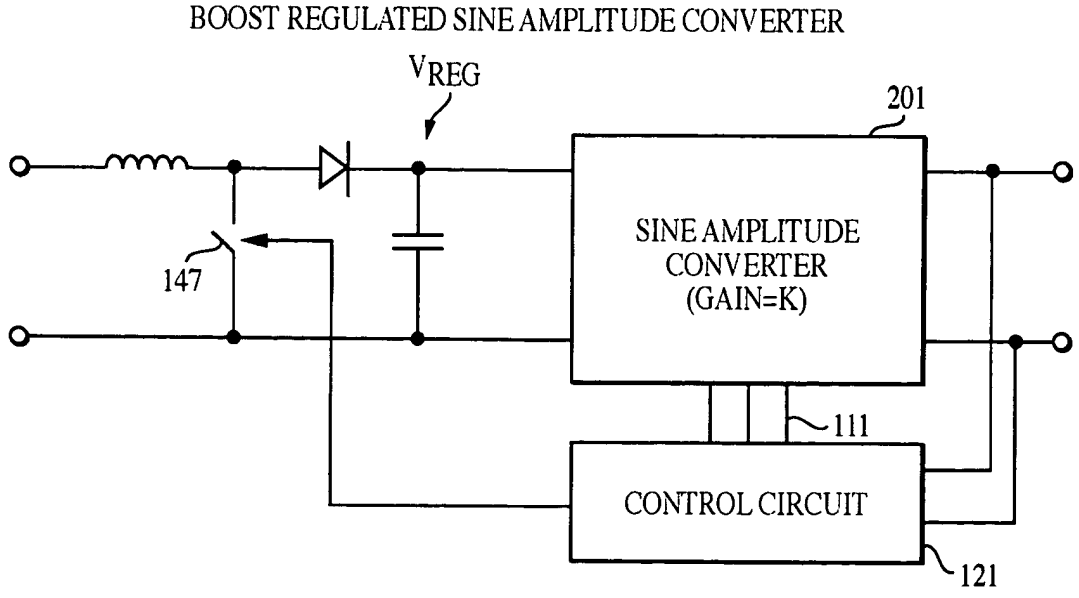


FIG. 29B

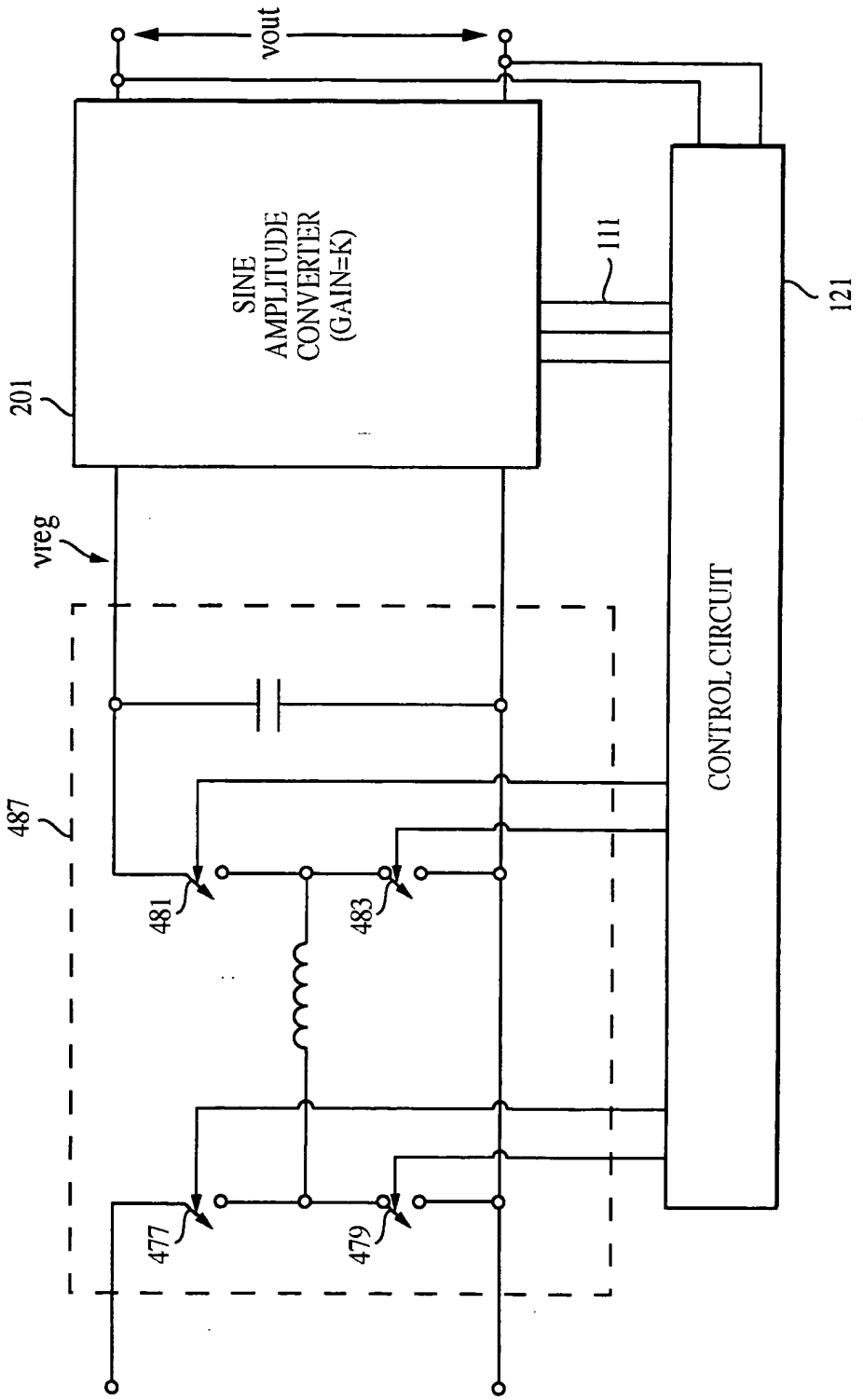

vout
SINE AMPLITUDE CONVERTER (GAIN=K)
111
121
201
vreg
CONTROL CIRCUIT
487
481
483
477
479

FIG. 29C

BOOT STRAP REGULATED DC-DC CONVERTER

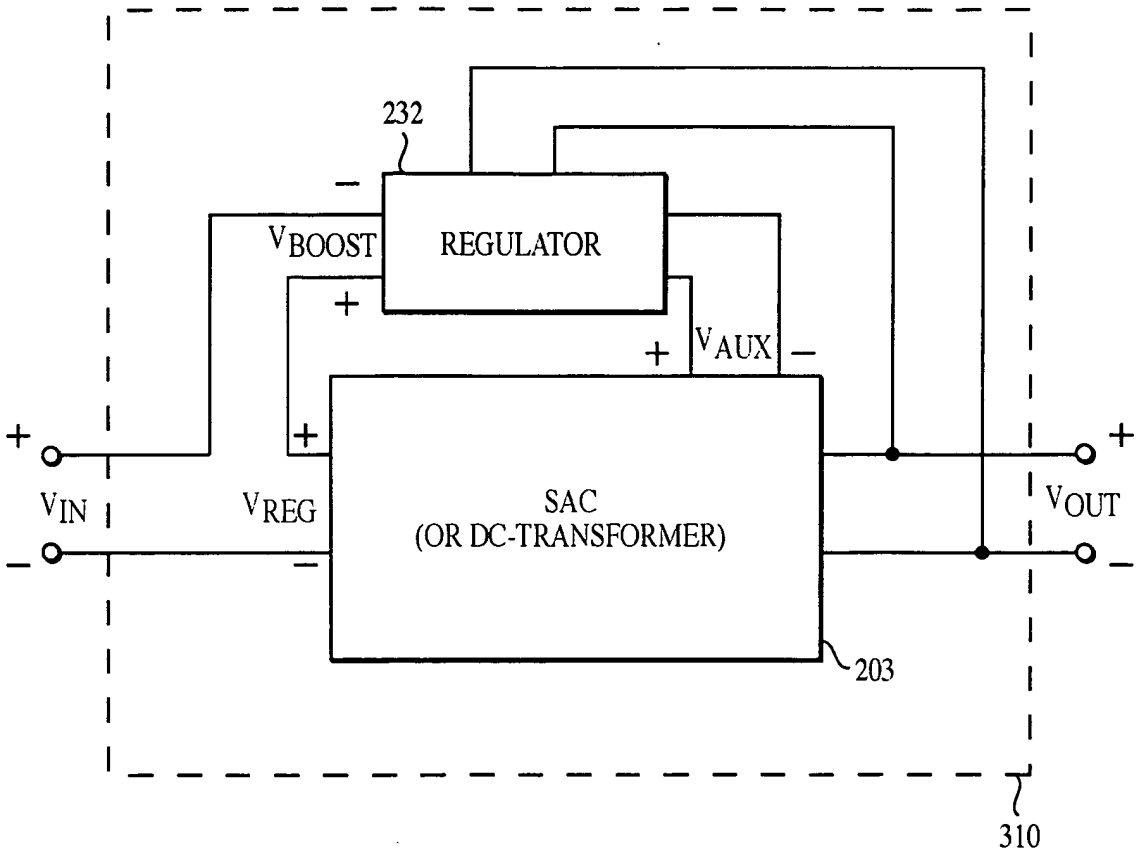


FIG. 30

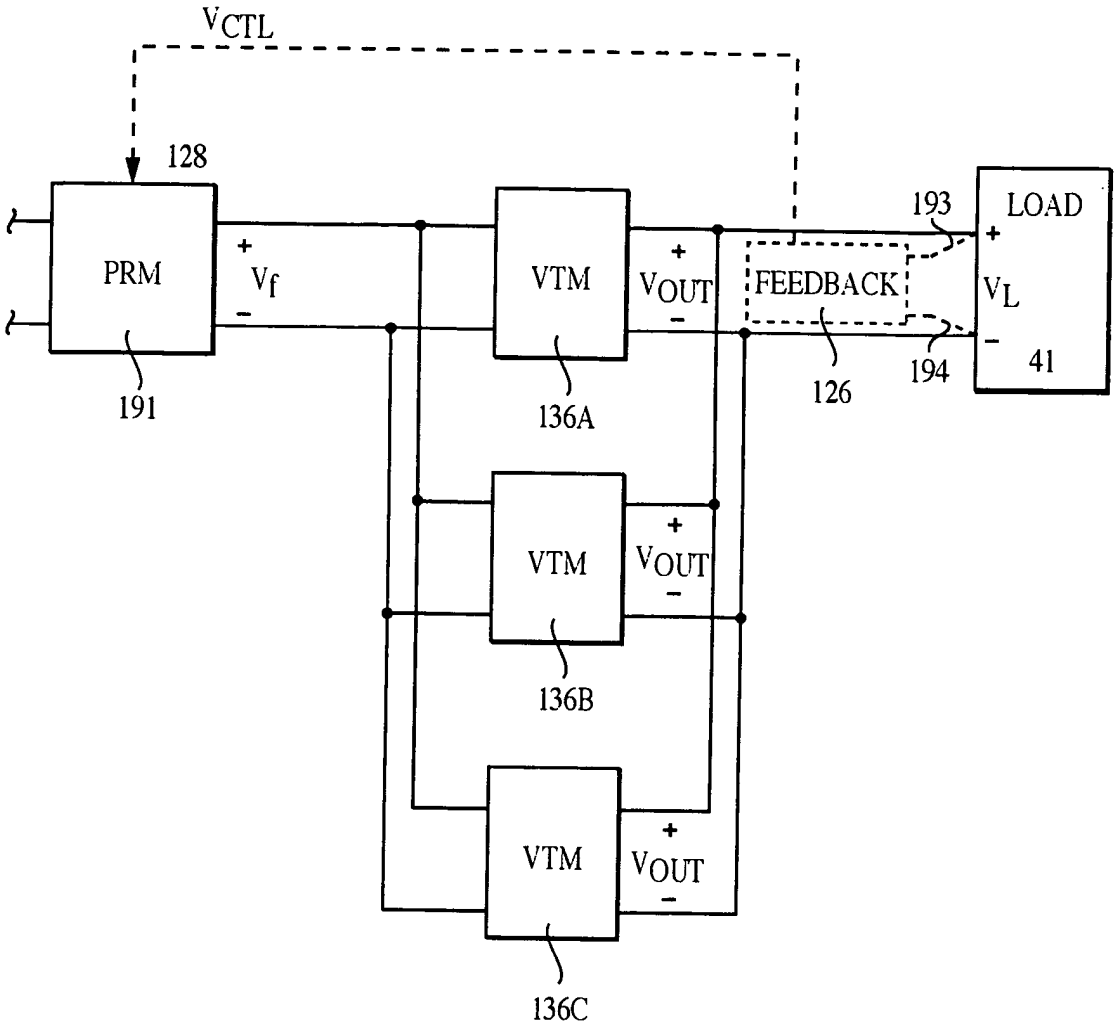

VCTL
128
PRM
+
Vf
−
191
VTM
+
VOUT
−
136A
193
LOAD
+
FEEDBACK
VL
−
126
194
41
VTM
+
VOUT
−
136B
VTM
+
VOUT
−
136C

FIG. 31

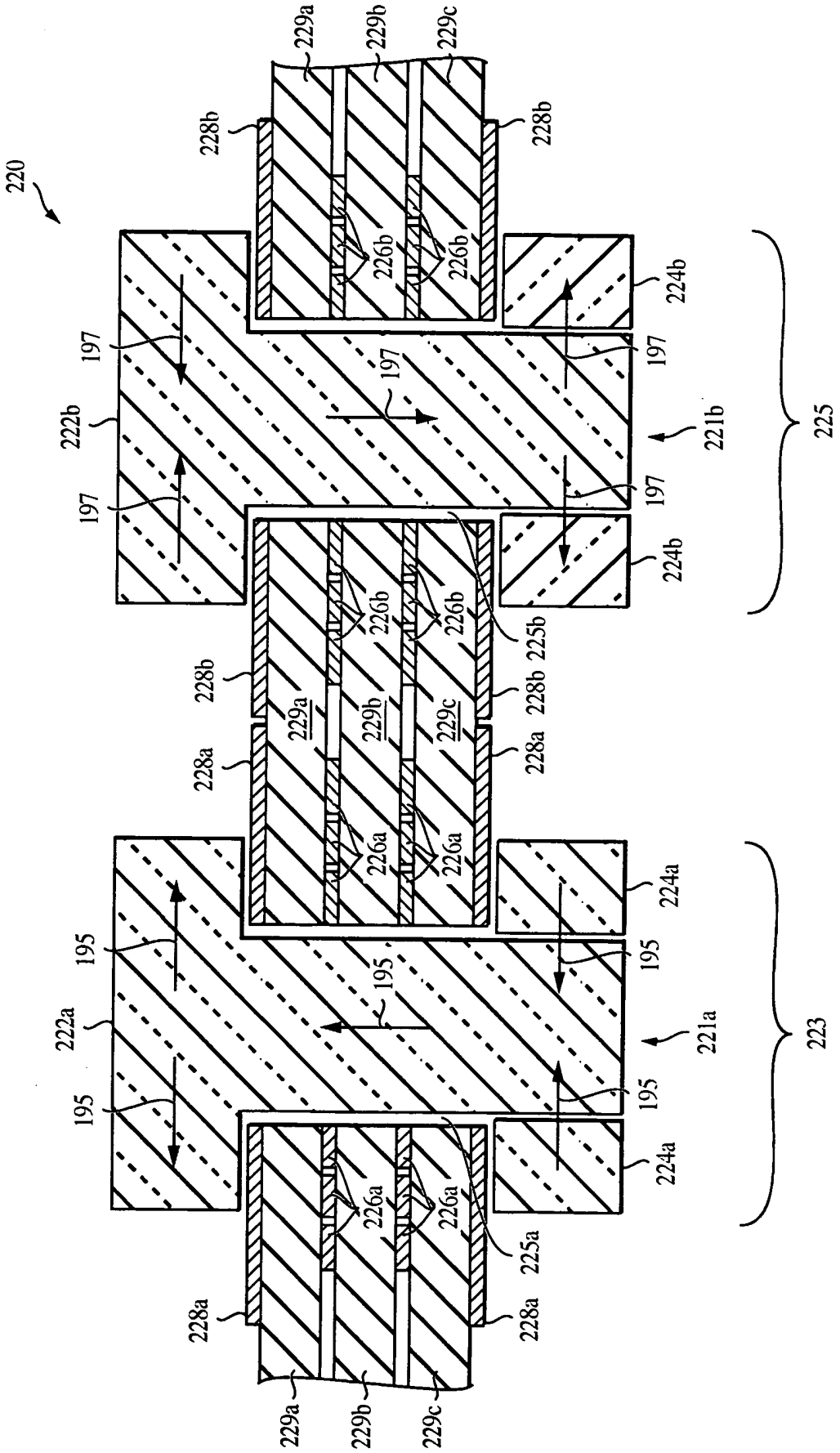

220
229a
229b
229c
228b
226b
224b
197
222b
221b
225
225b
228a
226a
224a
195
222a
221a
223

FIG. 32

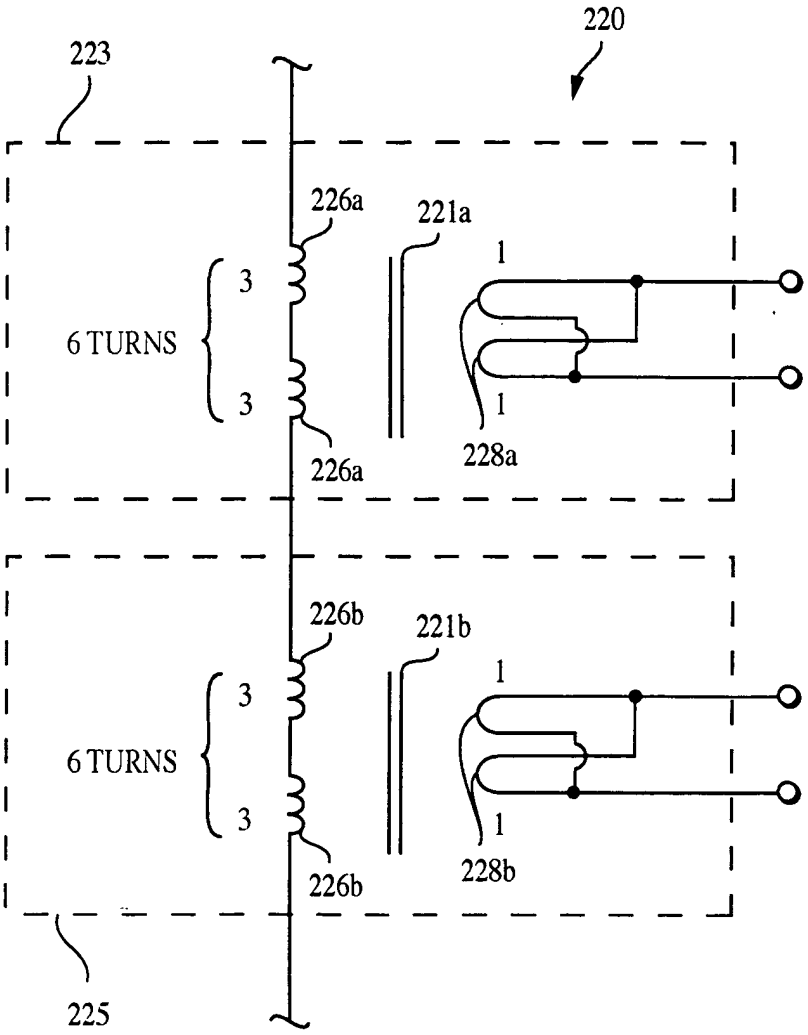

220
223
226a
221a
1
3
6 TURNS
3
1
226a
228a
226b
221b
1
3
6 TURNS
3
1
226b
228b
225

FIG. 33

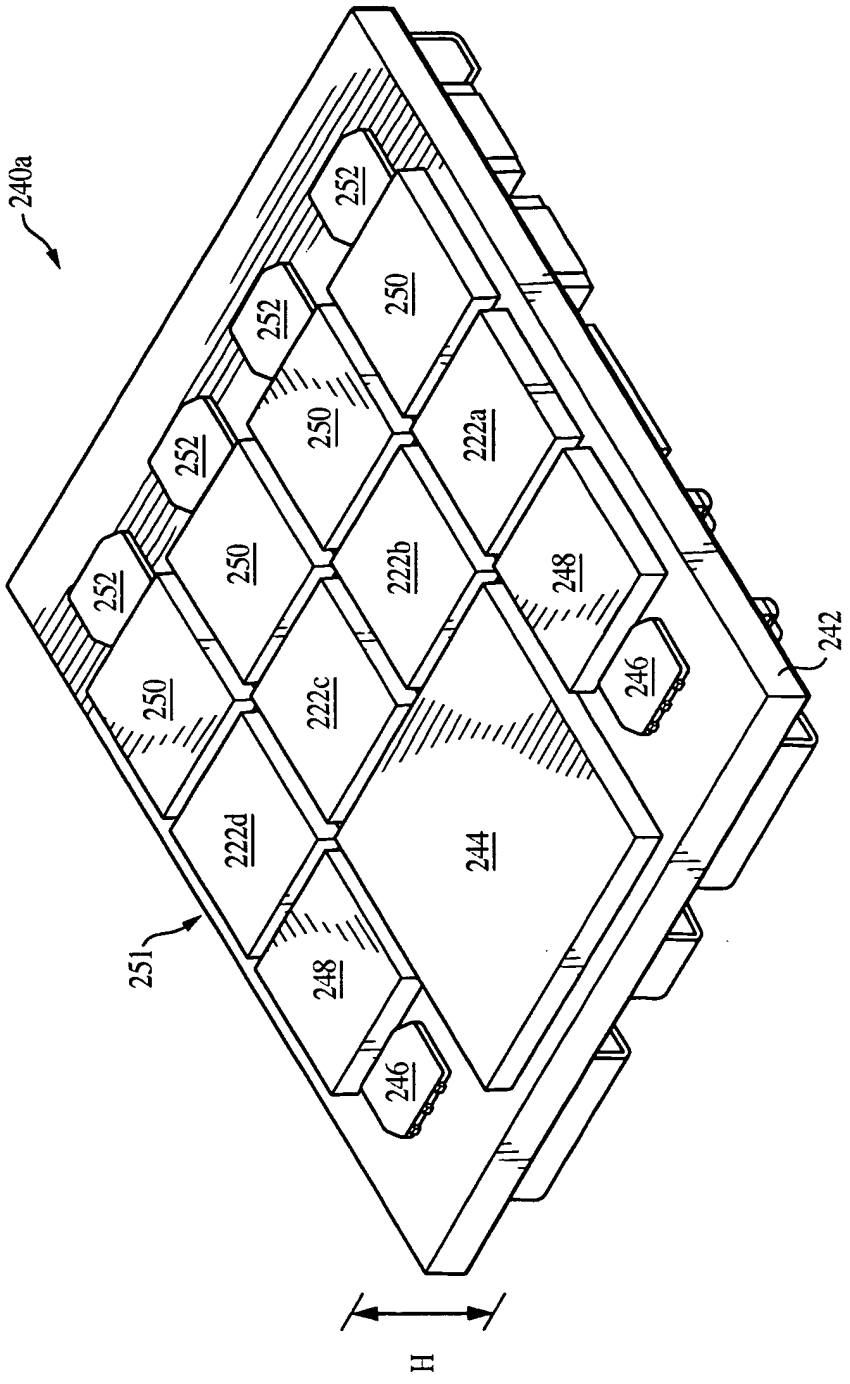


FIG. 34A

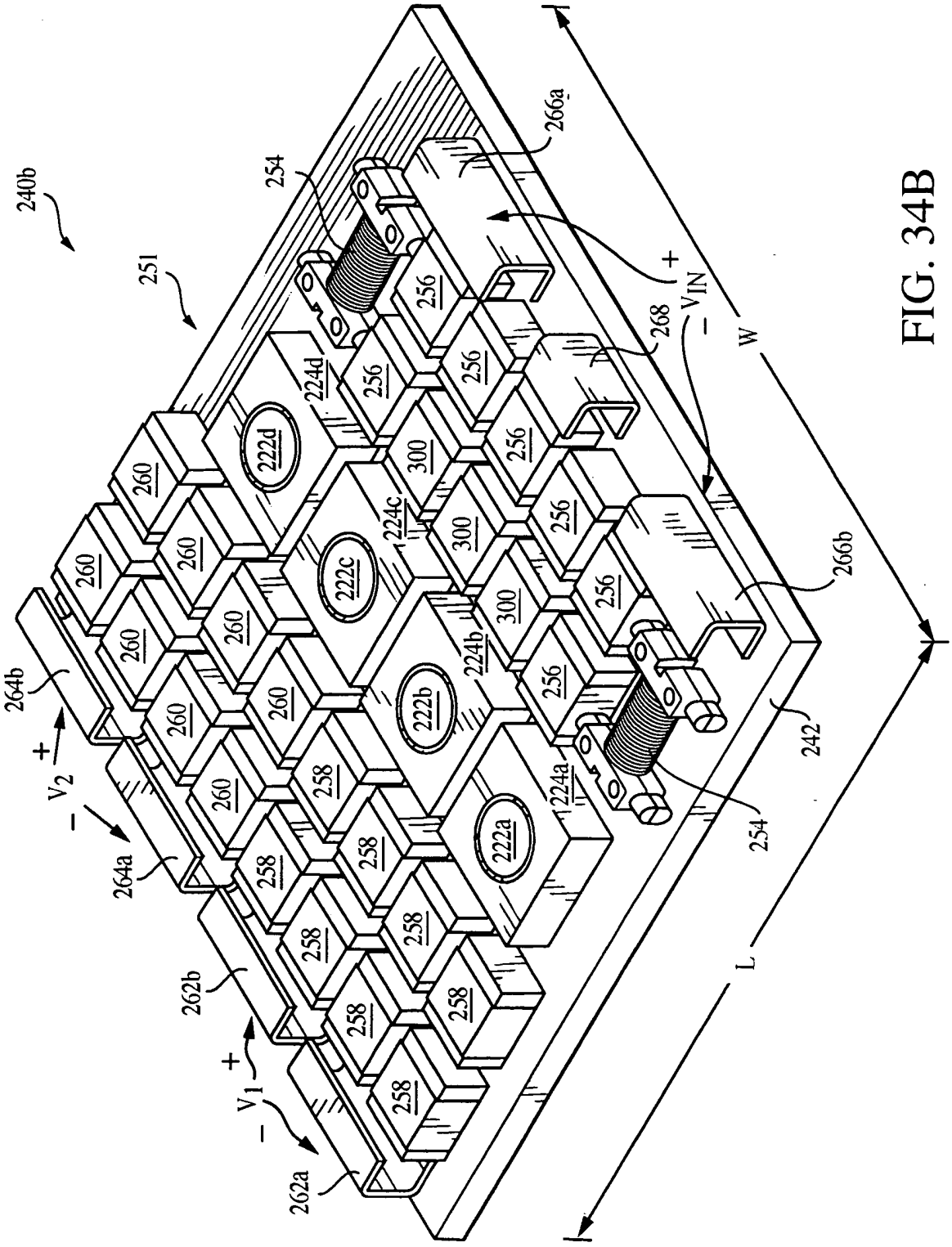

240b
251
254
266a
+ V_{IN} −
268
W
L
256
260
258
300
222a
222b
222c
222d
224a
224b
224c
224d
264b
264a
262b
262a
+ V_2 −
+ V_1 −
242

FIG. 34B

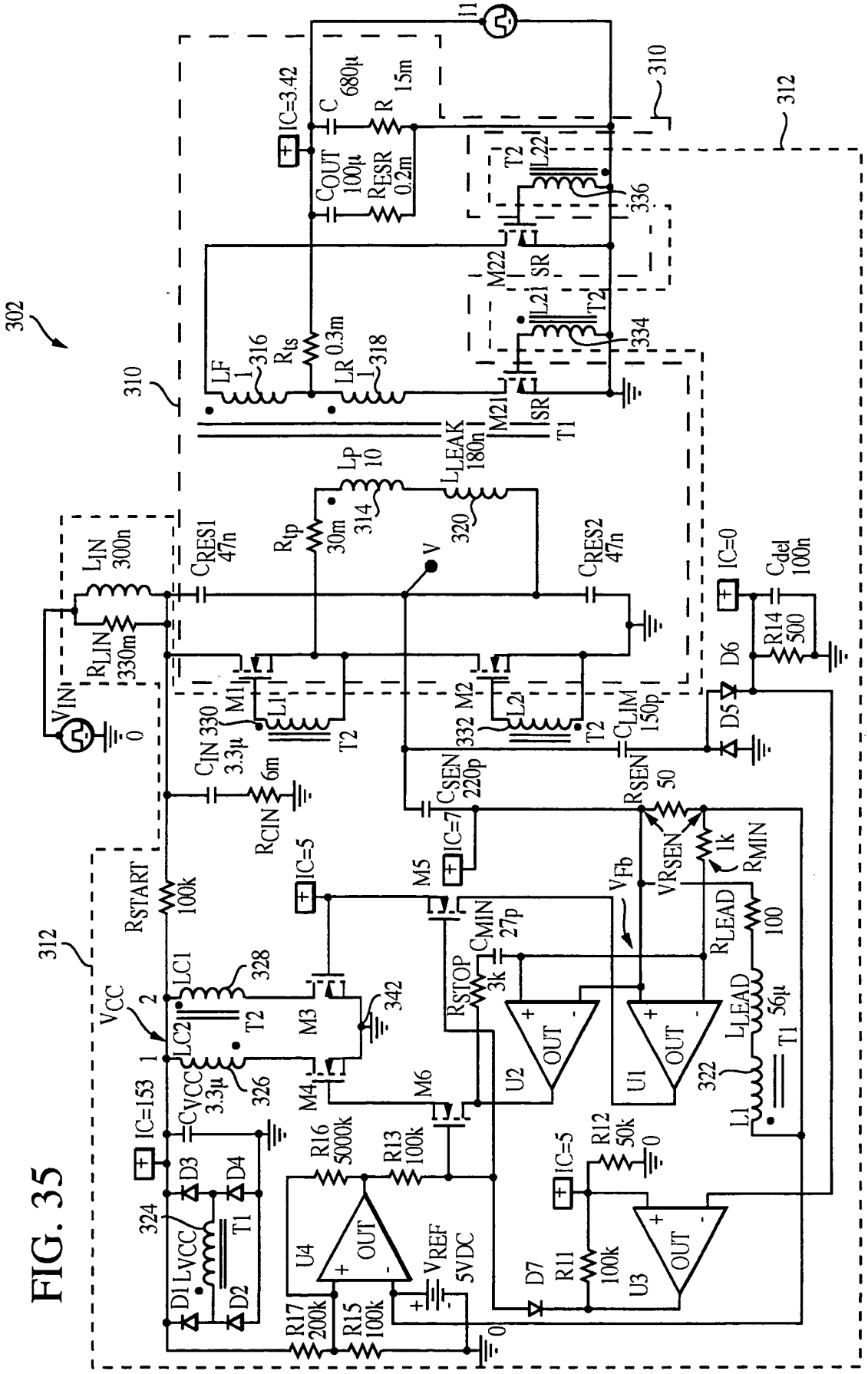

302
310
312
I1
C 680µ
R 15m
IC=3.42
COUT 100µ
RESR 0.2m
T2
L22
336
M22 SR
L21
T2
334
LF 316
Rls 0.3m
LR 318
M21 SR
T1
LLEAK 180n
LP 10
Rtp 30m
314
320
V
CRES1 47n
CRES2 47n
LIN 300n
RLIN 330m
VIN
0
IC=0
Cdel 100n
D6
R14 500
D5
M1 L1 T2
CIN 330 3.3µ
332 M2 L2 T2
CLIM 150p
CIN 6m
RCIN
CSEN 220p
IC=7
RSEN 50
IC=5
M5
VFb
VRSEN 1k
RMIN
RSTART 100k
CMIN 27p
RLEAD 100
RSTOP 3k
LC1 328
LC2 T2 M3 342
VCC 2
1
LCVCC 3.3µ 326
M4
M6
U2 OUT
U1 OUT
LLEAD 56µ
T1
322
L1
IC=153
CVCC 3.3µ
D3
D4
R16 5000k
R13 100k
R12 50k
0
IC=5
324
LVCC T1
D1
D2
U4 OUT
VREF 5VDC
D7
R11 100k
U3 OUT
R17 200k
R15 100k
0

FIG. 35

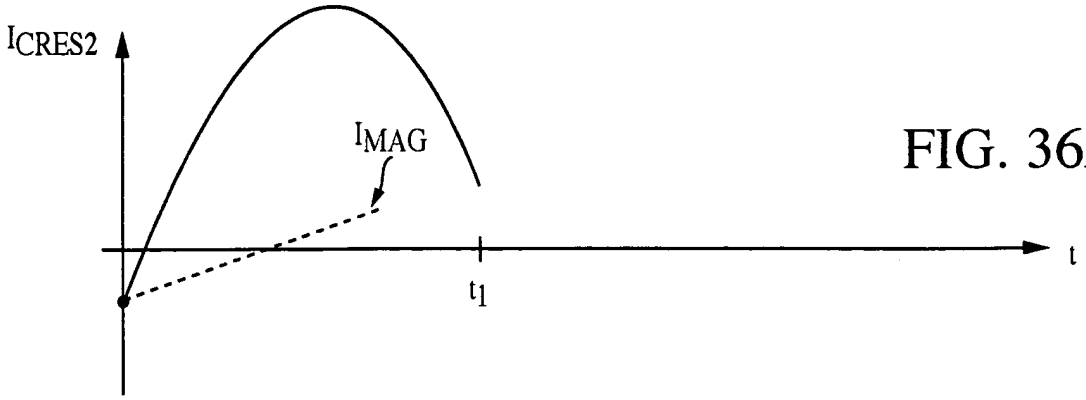


FIG. 36A

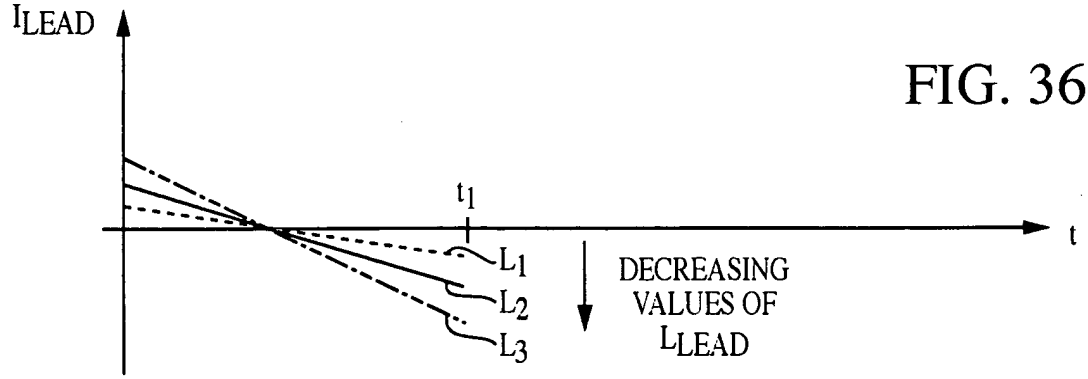


FIG. 36B

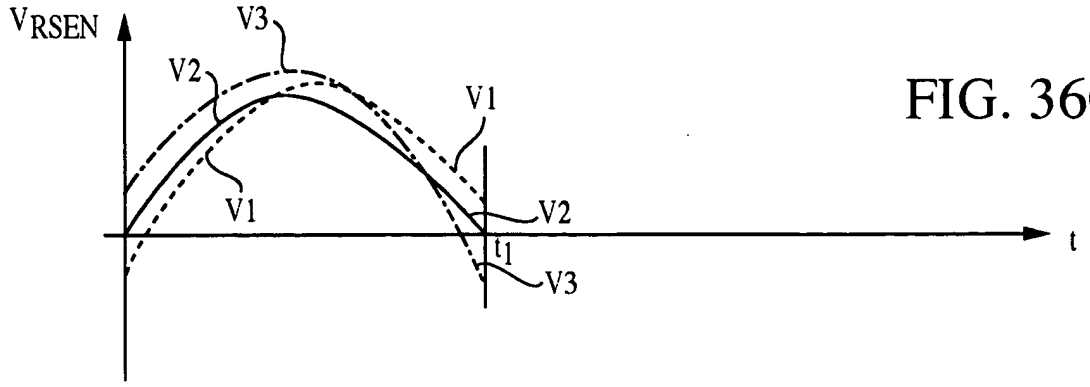


FIG. 36C

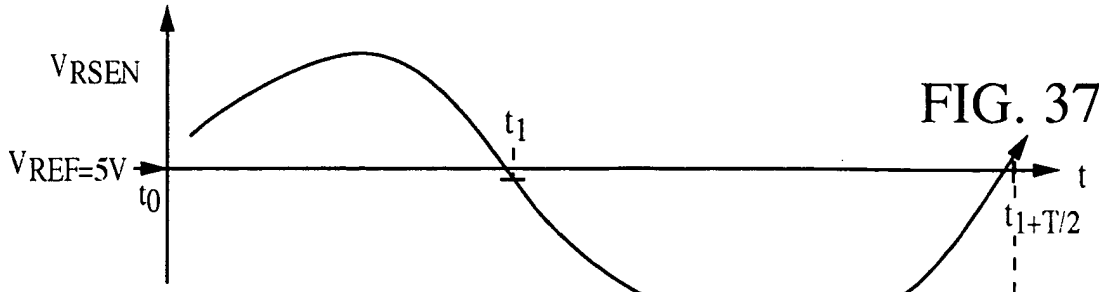


FIG. 37A

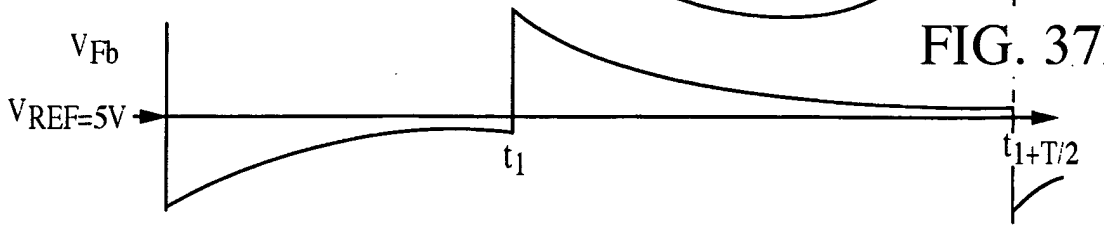


FIG. 37B

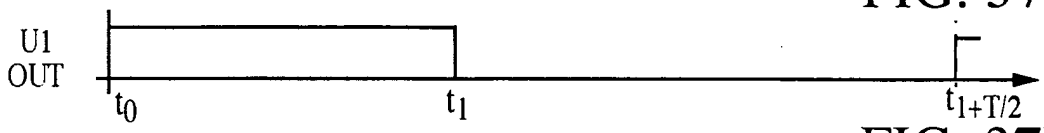


FIG. 37C

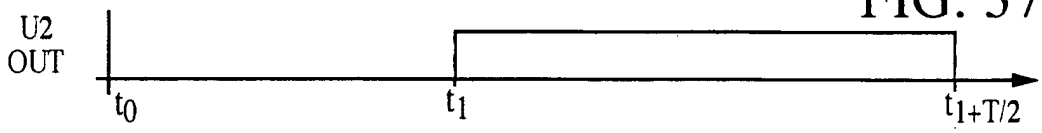


FIG. 37D

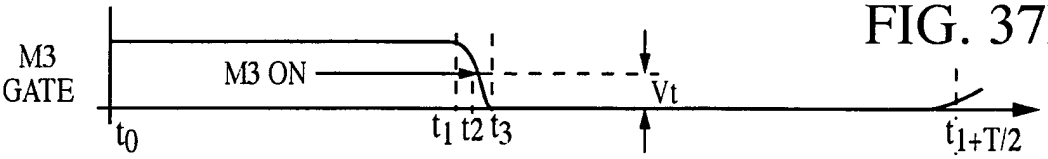


FIG. 37E

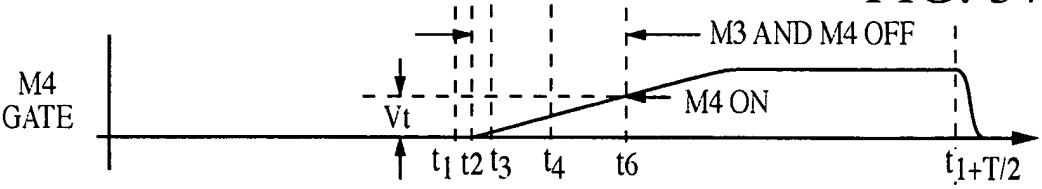


FIG. 37F

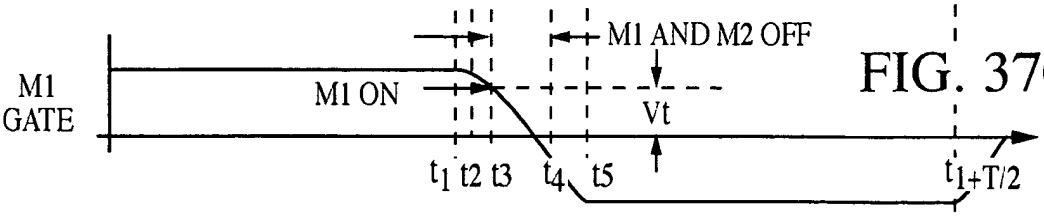


FIG. 37G

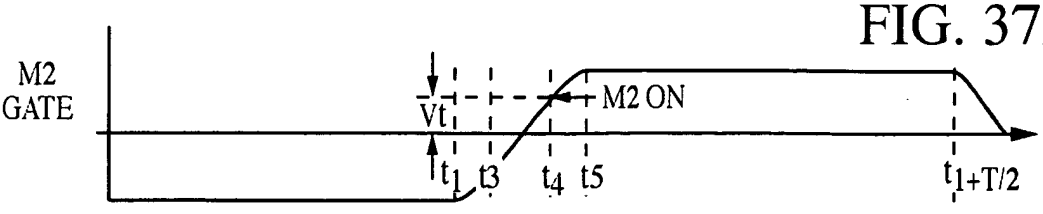


FIG. 37H

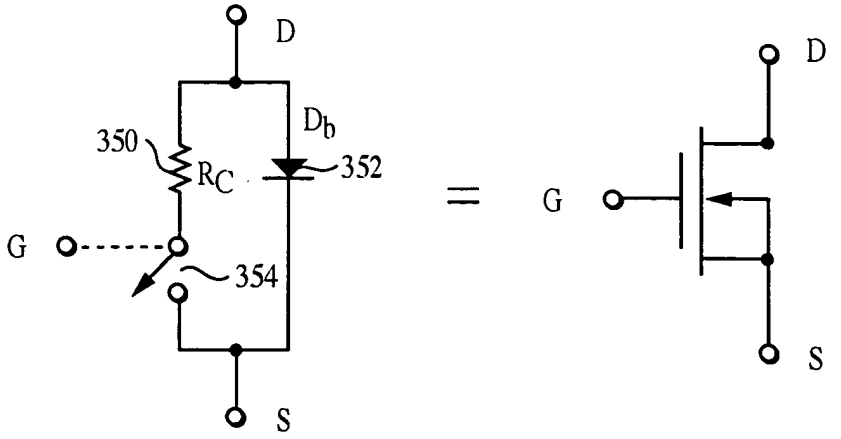


FIG. 38

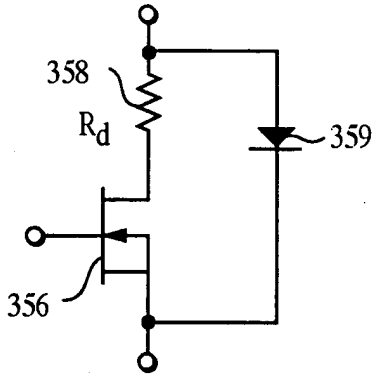


FIG. 39A

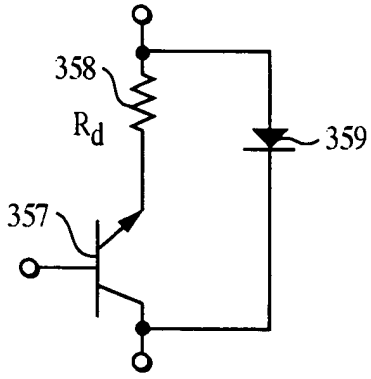


FIG. 39B

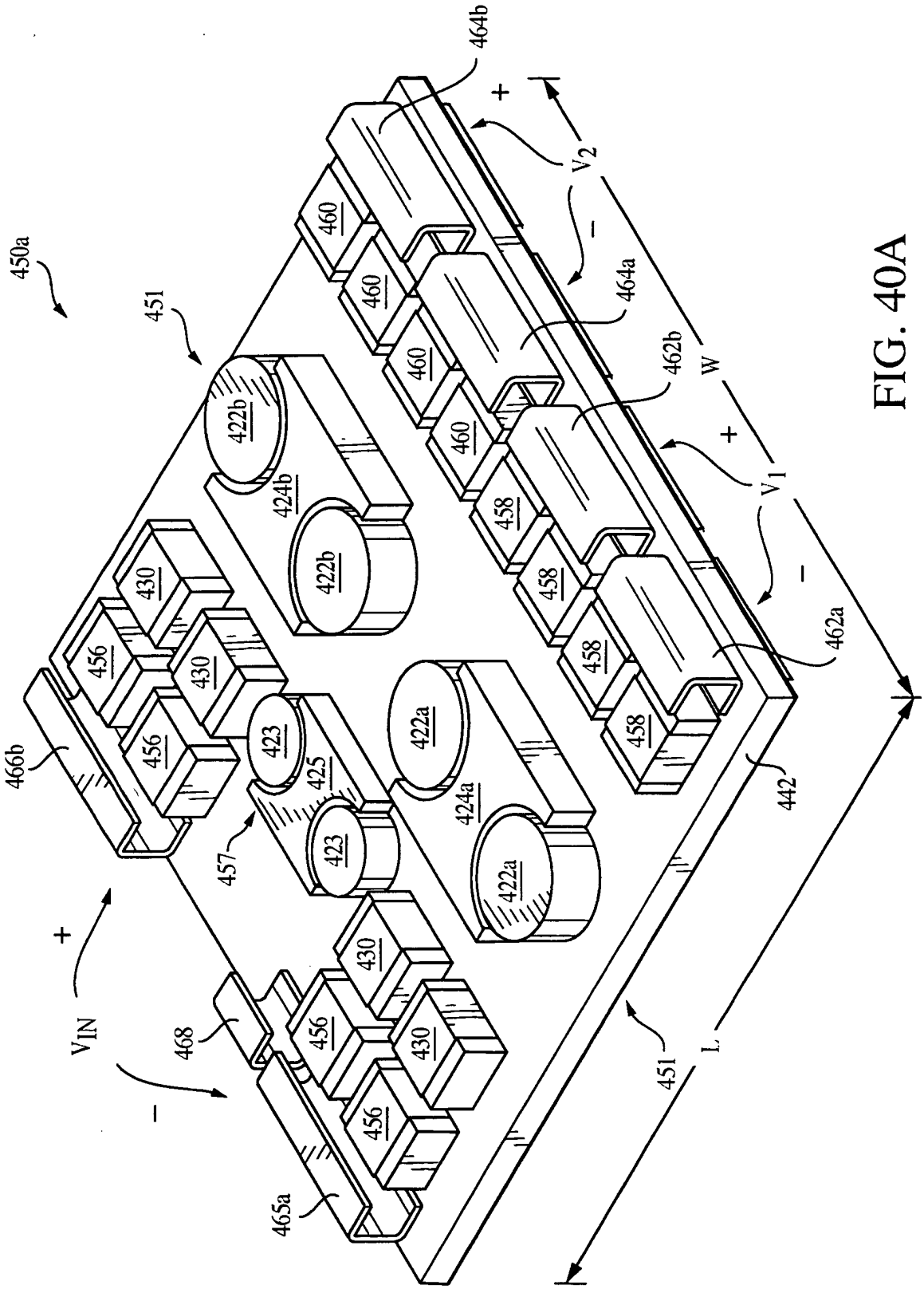

450a
451
464b
460
464a
462b
462a
422b
424b
422a
424a
423
425
457
430
456
458
466b
468
465a
442
V_{IN}
V_1
V_2
W
L
+
–

FIG. 40A

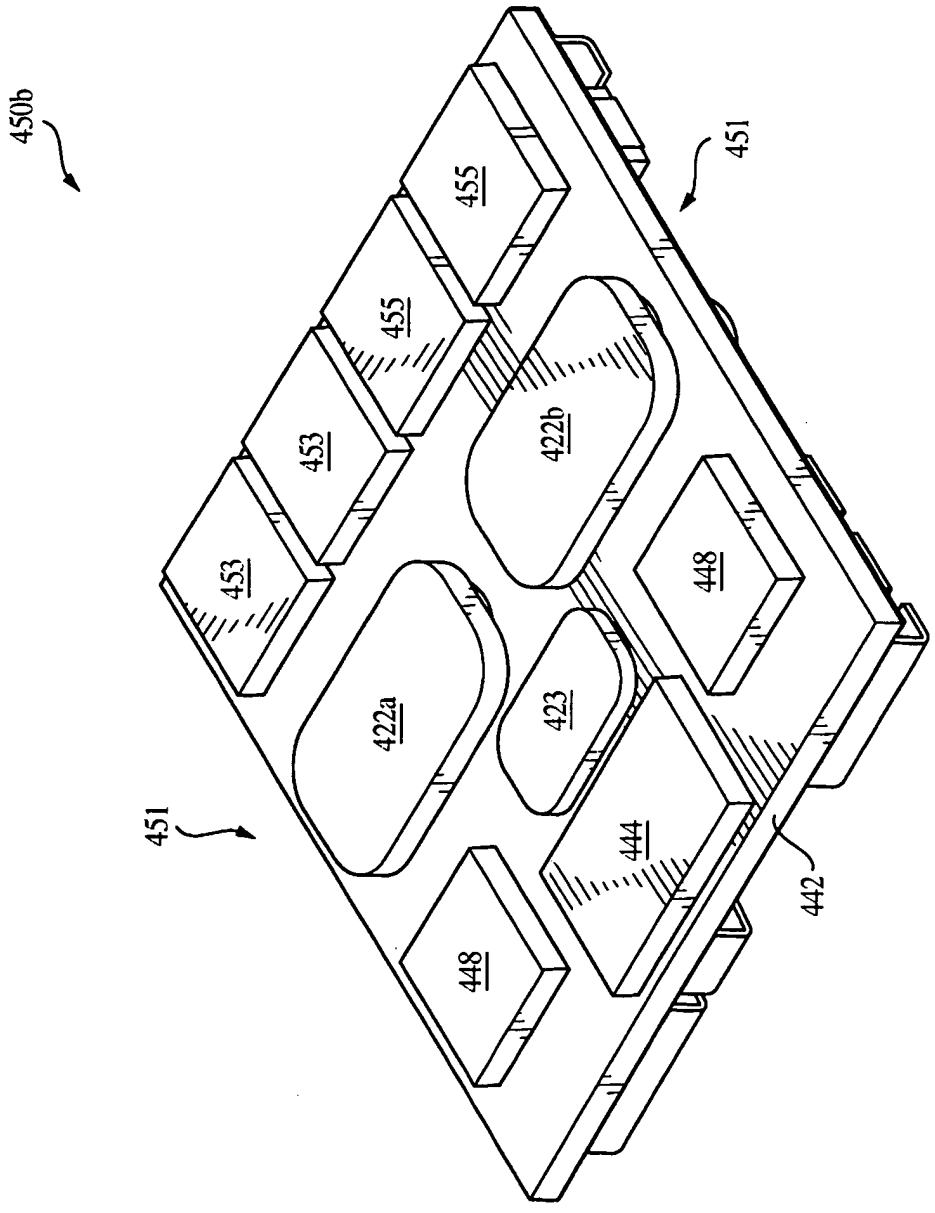


FIG. 40B

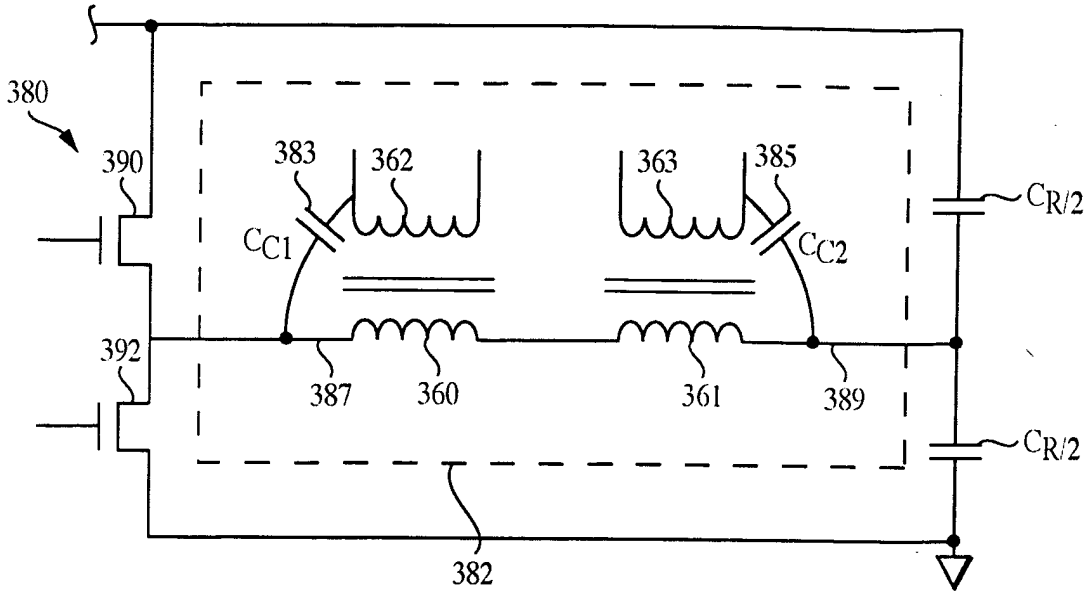

380
390
383
362
363
385
C_{C1}
C_{C2}
$C_{R/2}$
392
387
360
361
389
$C_{R/2}$
382

FIG. 41

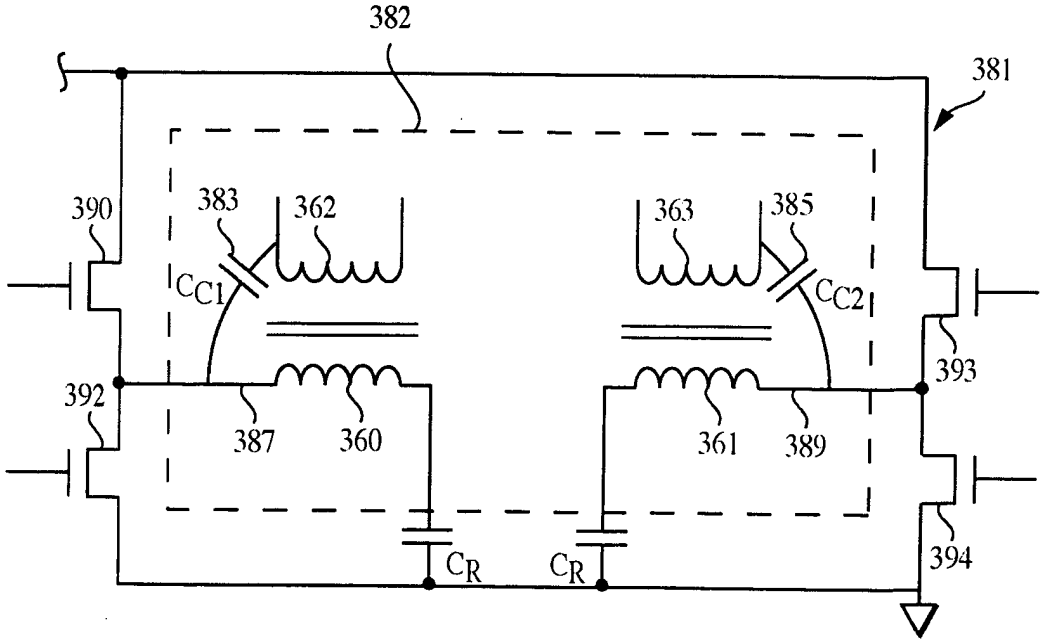

382
381
390
383
362
363
385
C_{C1}
C_{C2}
392
393
387
360
361
389
C_R
C_R
394

FIG. 42

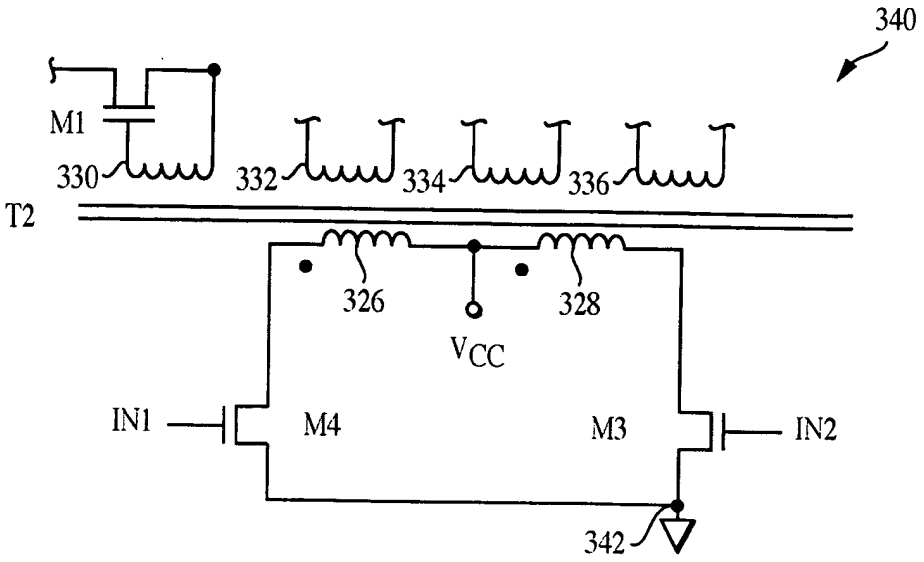

340
M1
330
332
334
336
T2
326
328
VCC
IN1
M4
M3
IN2
342

FIG. 43

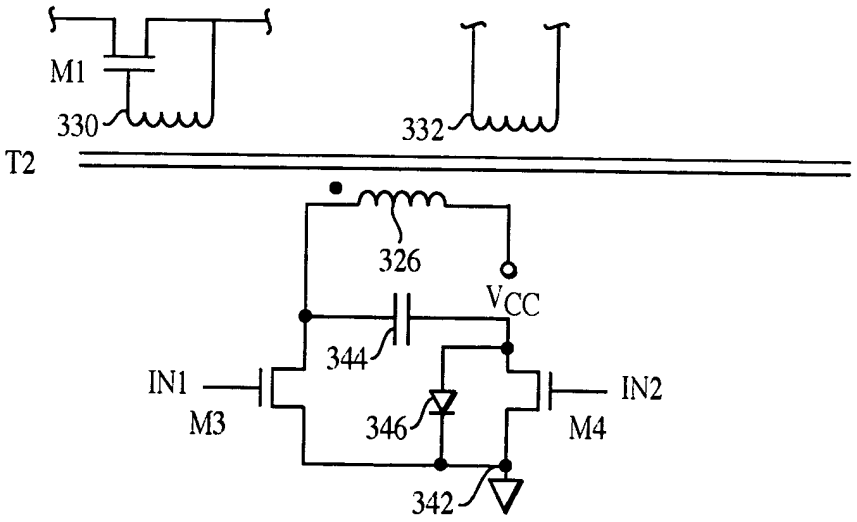

M1
330
332
T2
326
VCC
344
IN1
M3
346
IN2
M4
342

FIG. 44

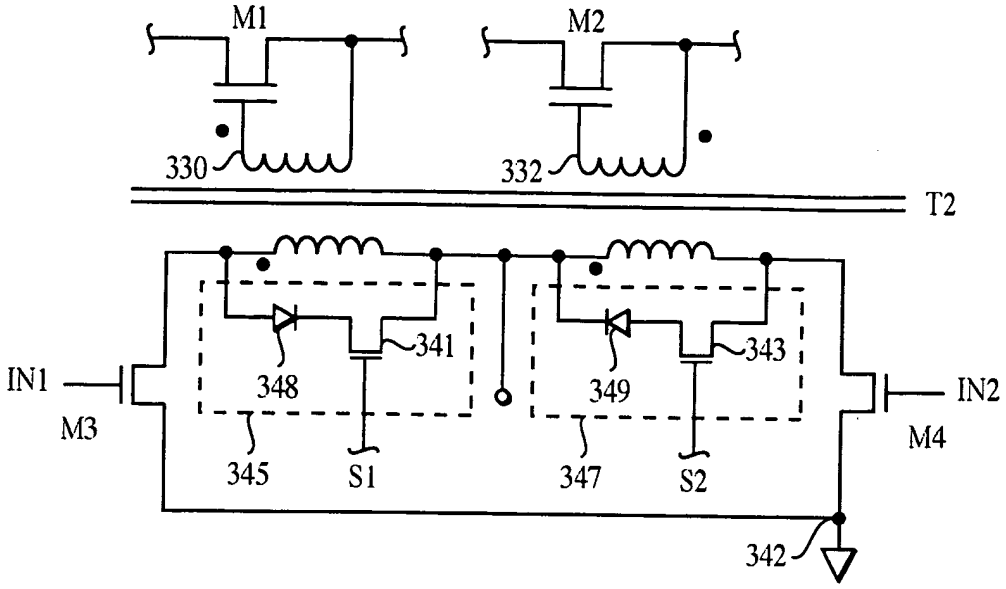


FIG. 45

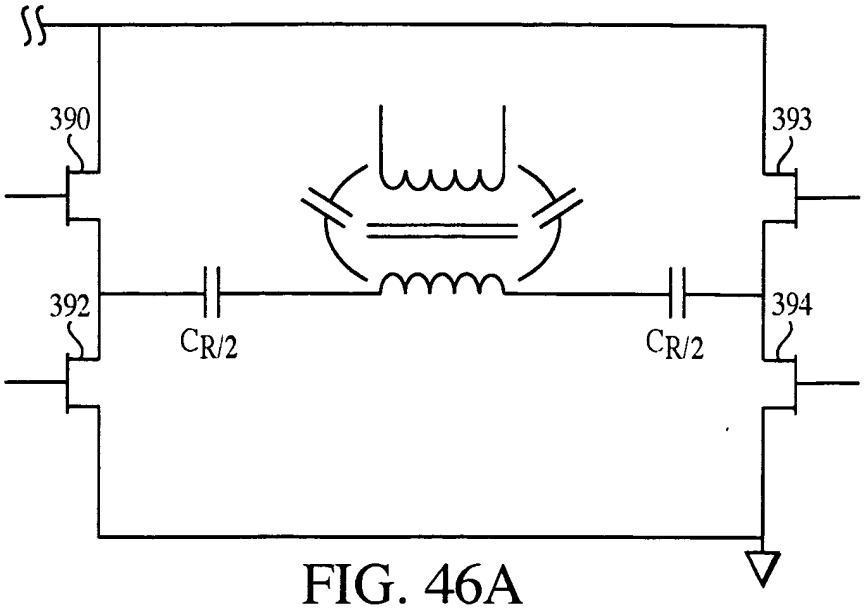


FIG. 46A

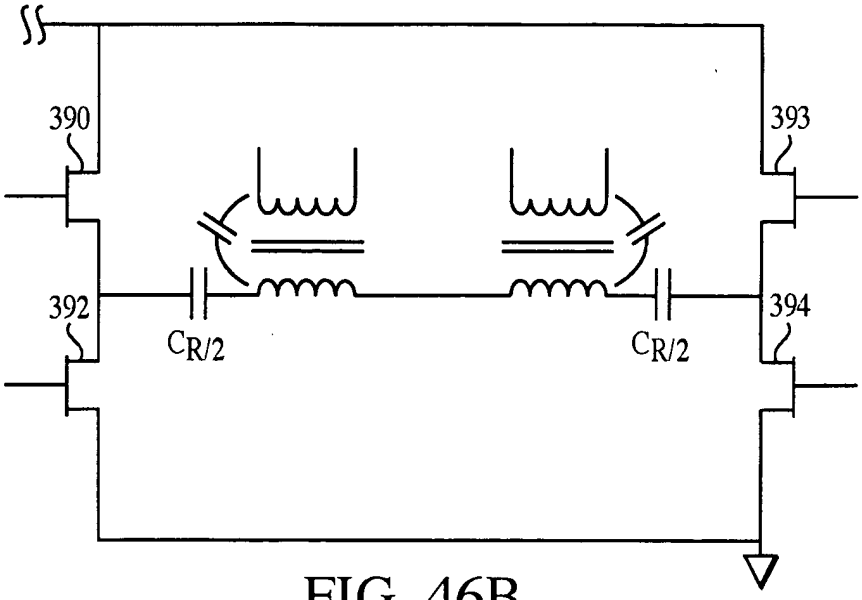


FIG. 46B

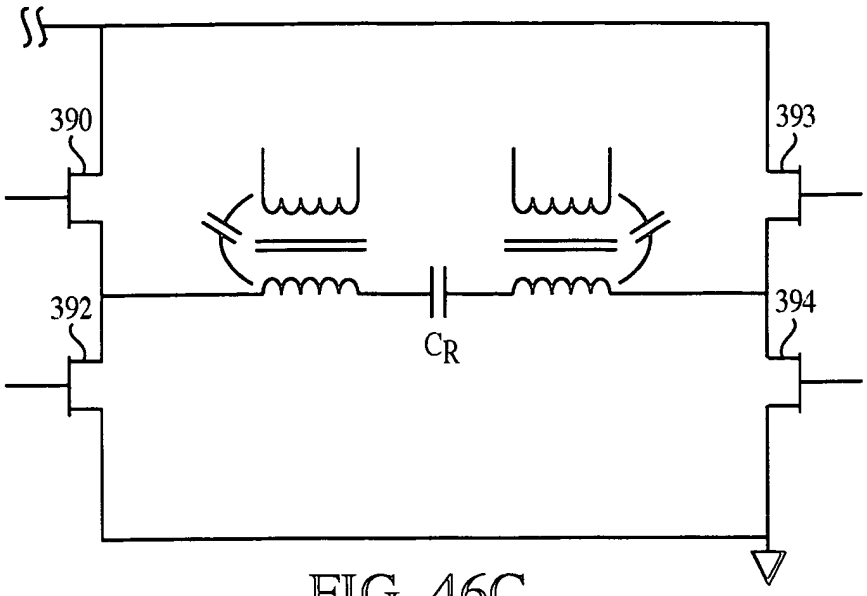


FIG. 46C

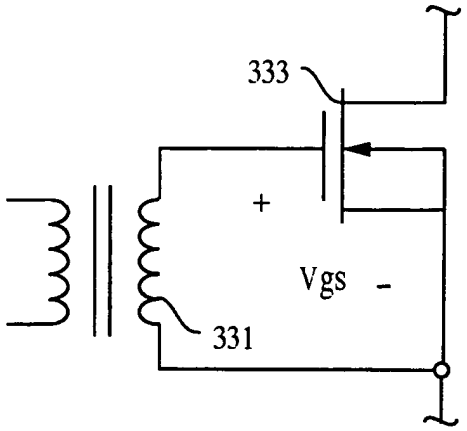


FIG. 47A

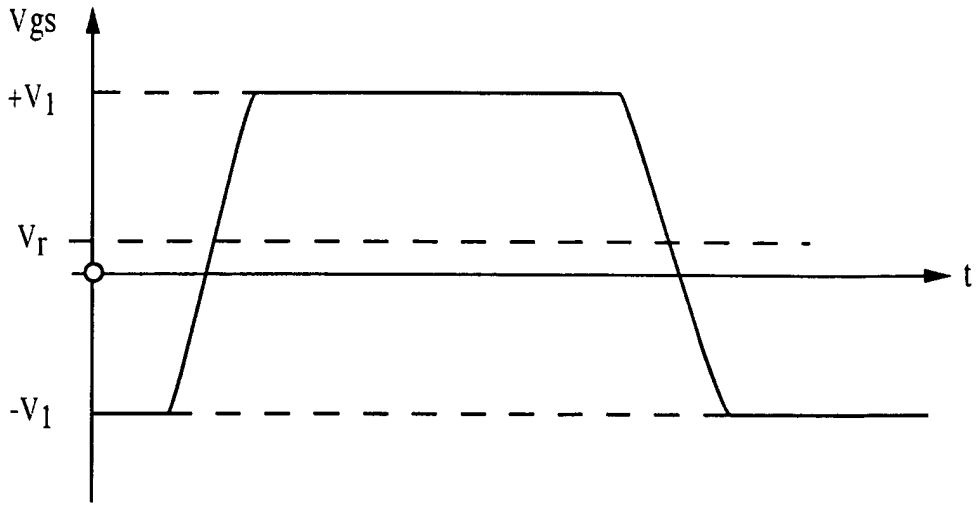


FIG. 47B

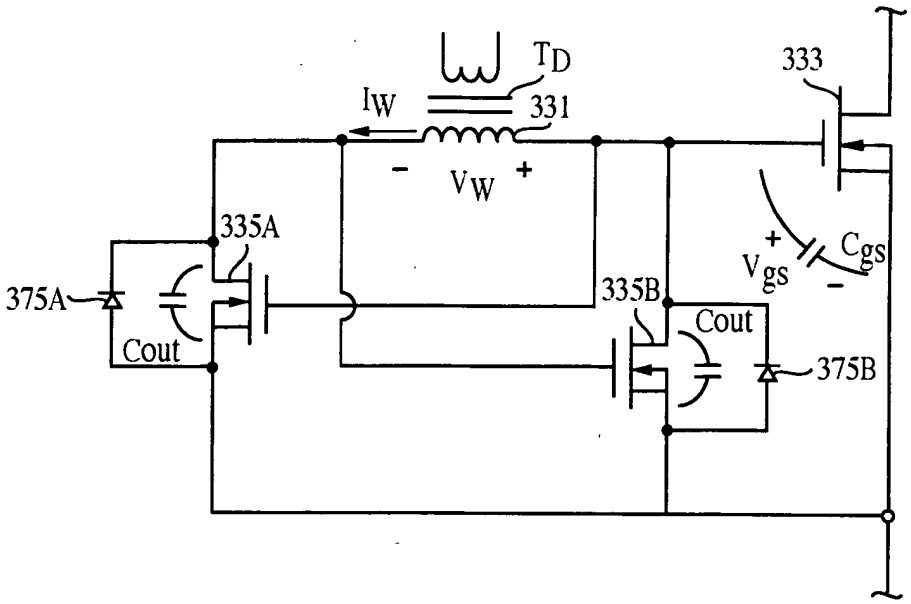


FIG. 48A

FIG. 48B

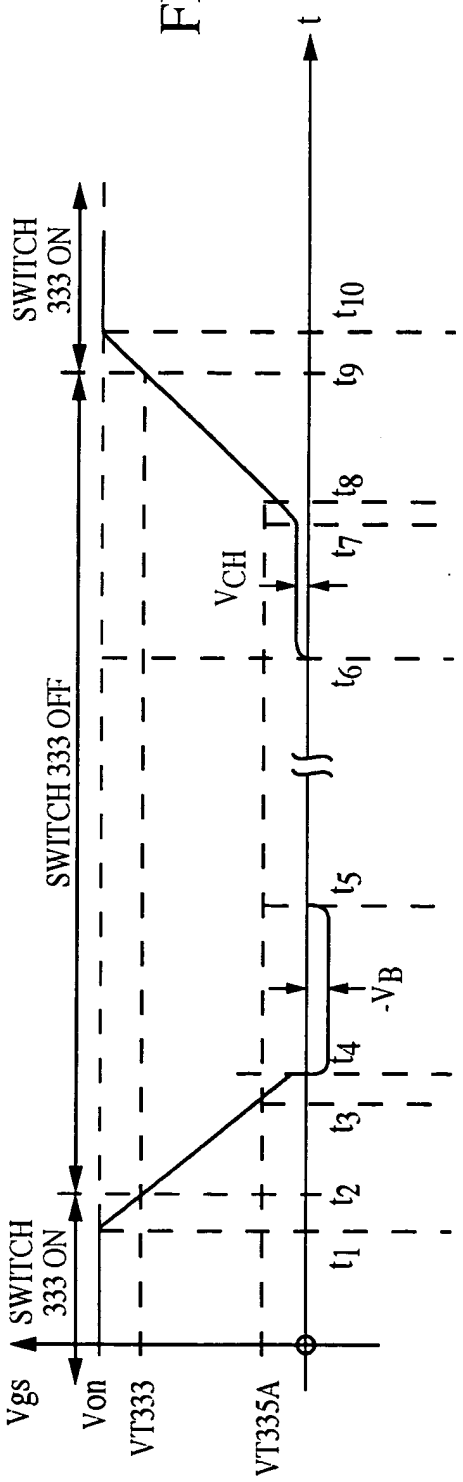
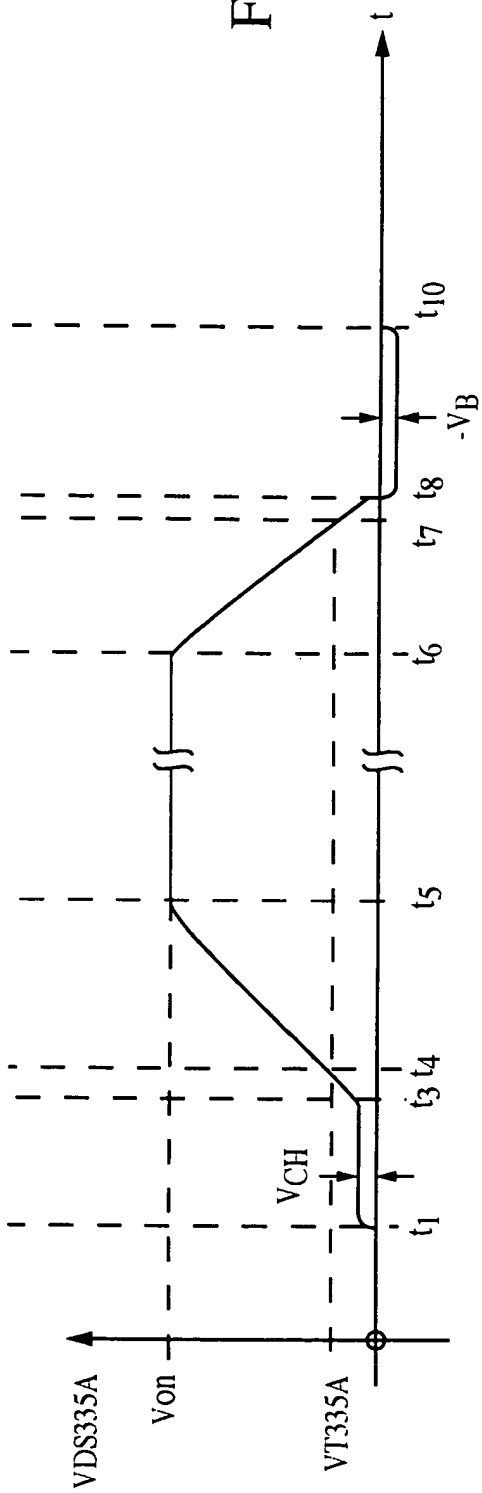


FIG. 48C



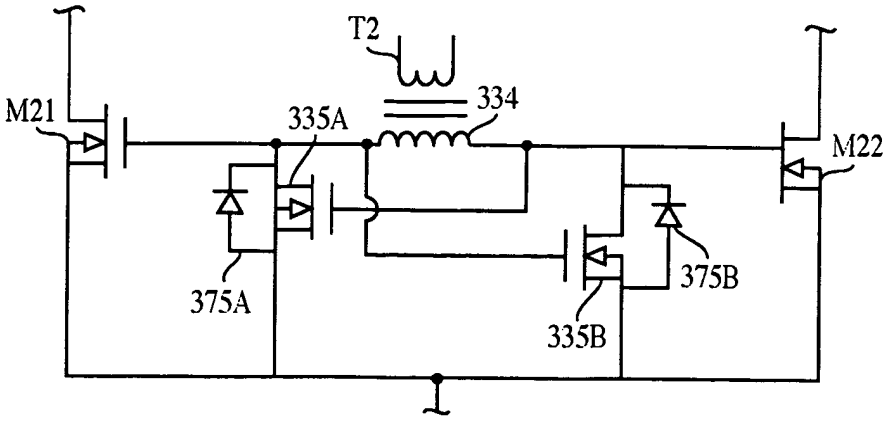

T2
334
M21
335A
M22
375A
375B
335B

FIG. 49

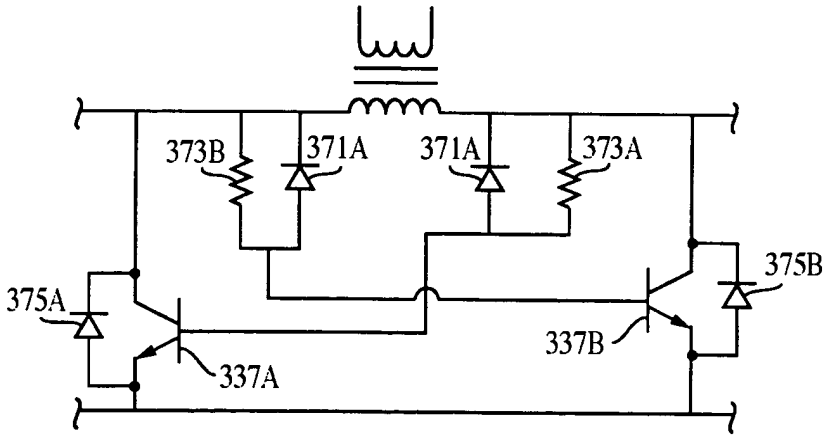

373B
371A
371A
373A
375B
375A
337B
337A

FIG. 50

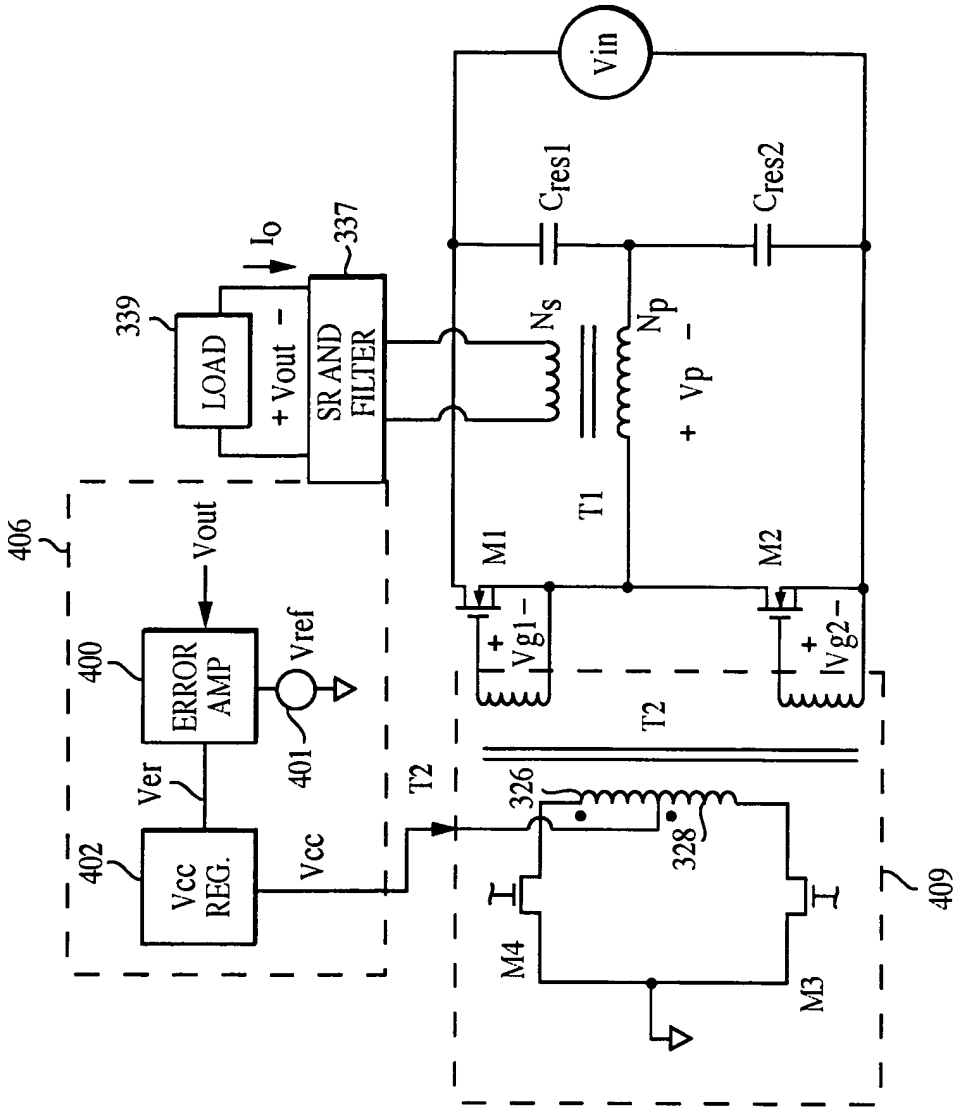

Vin
Cres1
Cres2
Io
337
339
LOAD
+ Vout -
SR AND FILTER
Ns
Np
+ Vp -
T1
M1
M2
406
Vout
400
ERROR AMP
Vref
401
+ Vg1 -
+ Vg2 -
T2
Ver
402
Vcc REG.
Vcc
326
328
M4
M3
409

FIG. 51

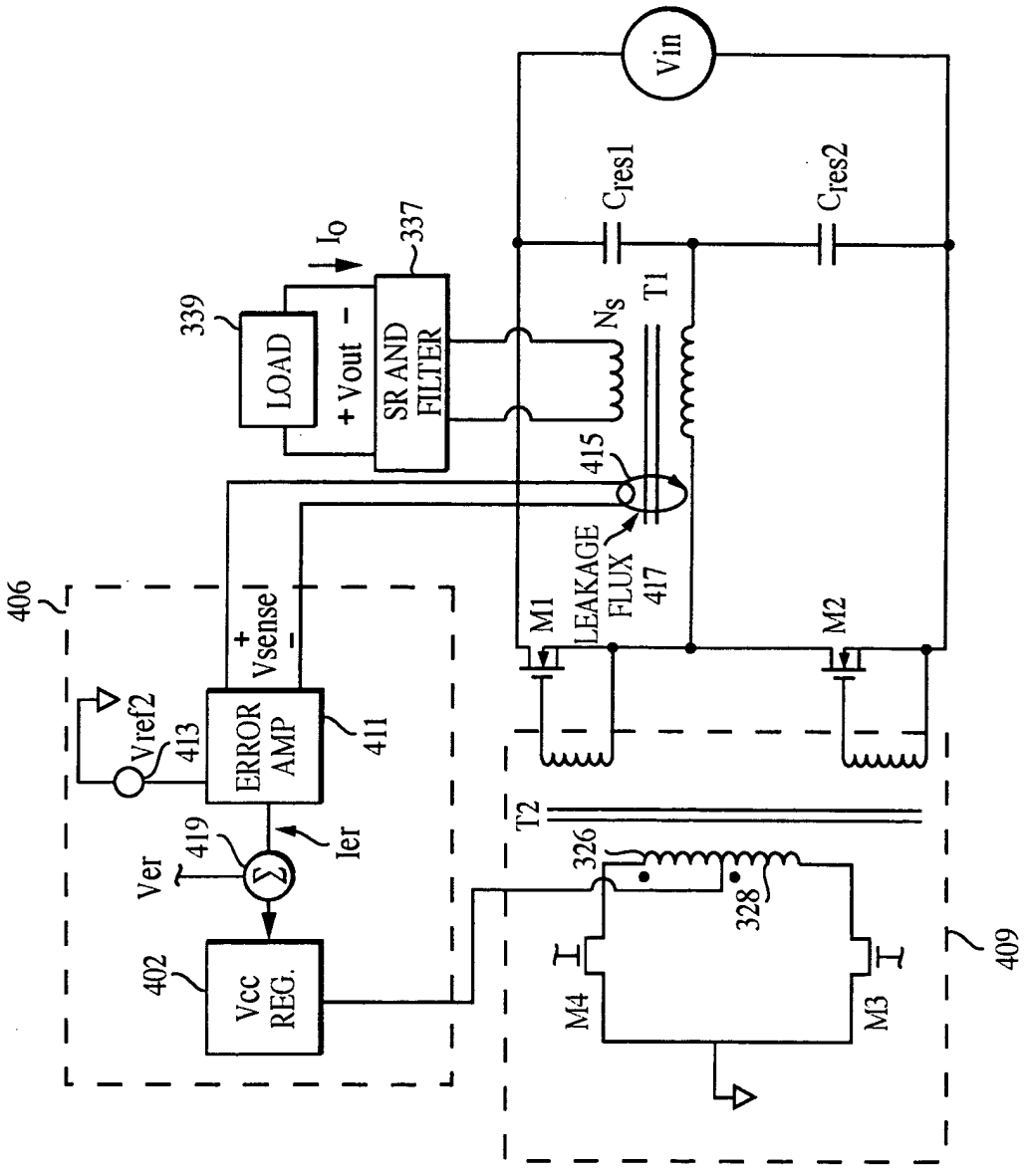

Vin
C_{res1}
C_{res2}
I_O
337
339
LOAD
+ Vout −
SR AND FILTER
N_S
T1
415
LEAKAGE FLUX 417
M1
M2
406
+ Vsense −
Vref2
413
ERROR AMP
411
Ver
419
Ier
402
Vcc REG.
T2
326
328
M4
M3
409

FIG. 52

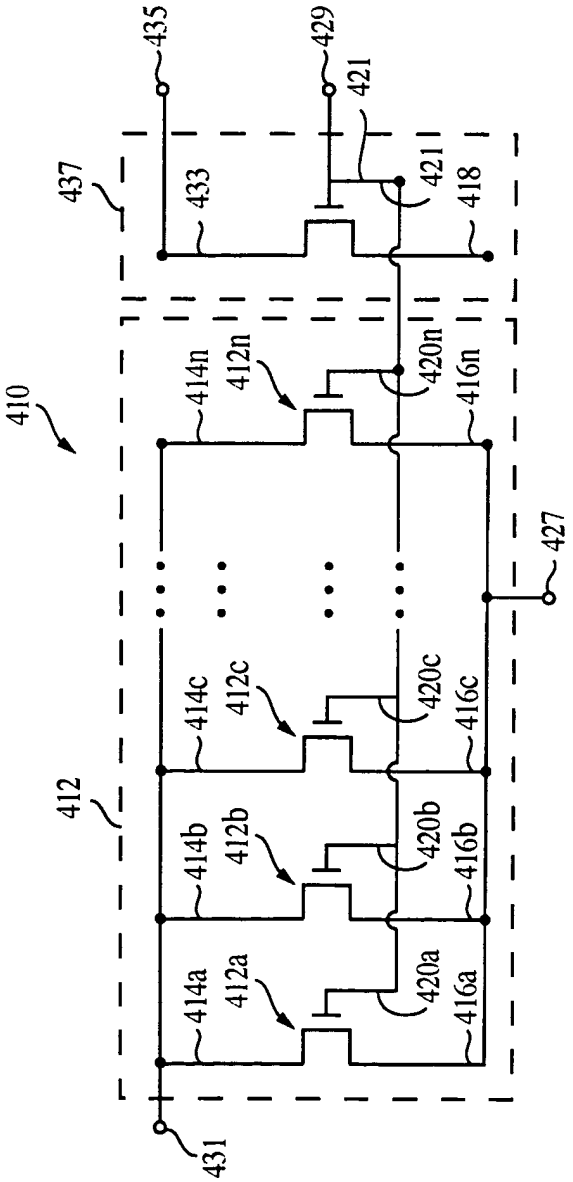

435
429
421
437
433
421
418
410
414n
412n
420n
416n
427
414c
412c
420c
416c
412
414b
412b
420b
416b
414a
412a
420a
416a
431

FIG. 53

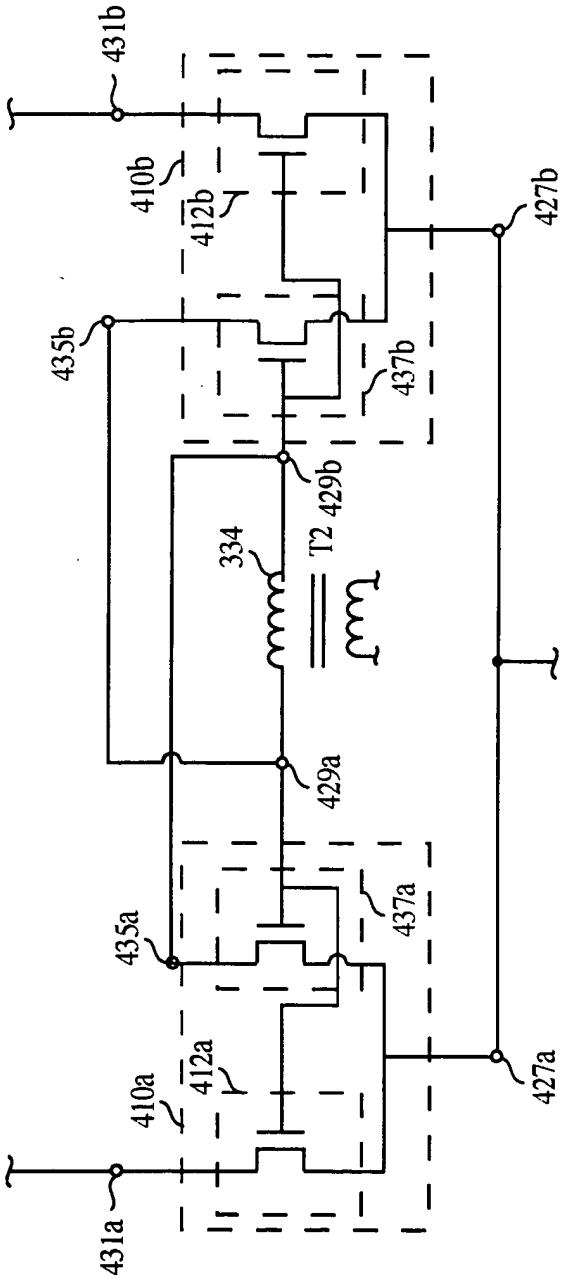

431b
410b
412b
427b
435b
437b
429b
T2
334
429a
435a
437a
427a
412a
410a
431a

FIG. 54

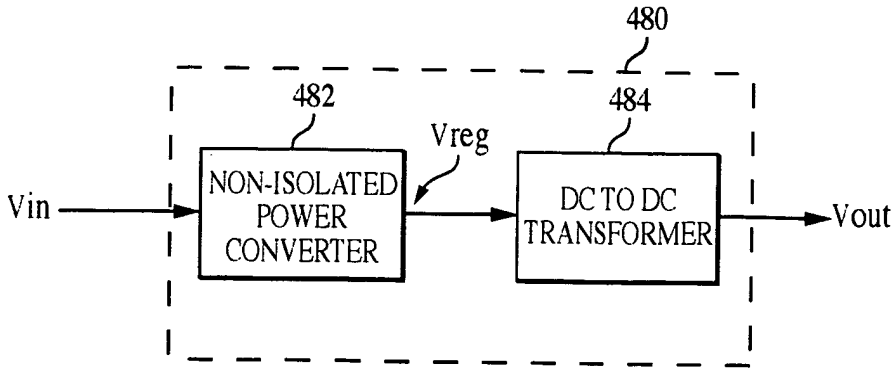


FIG. 55A

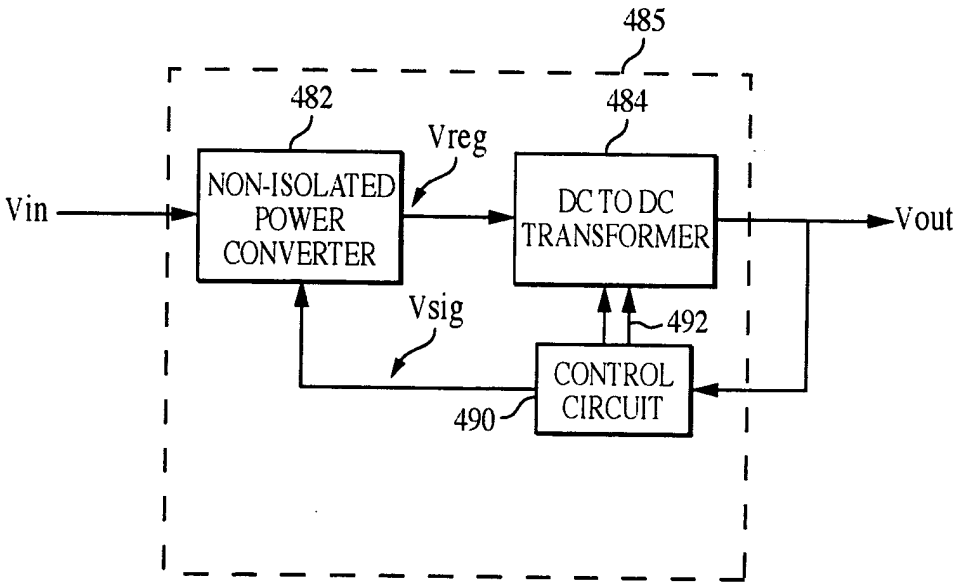


FIG. 55B

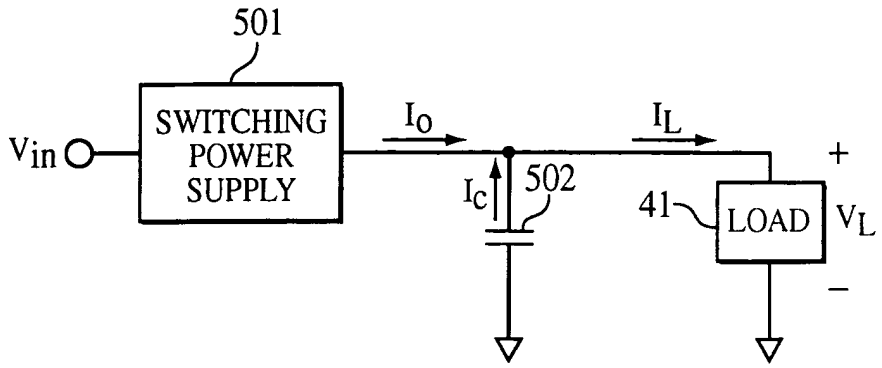

501
SWITCHING
POWER
SUPPLY
Vin
Io
IL
Ic
502
41
LOAD
VL
+
–

FIG. 56

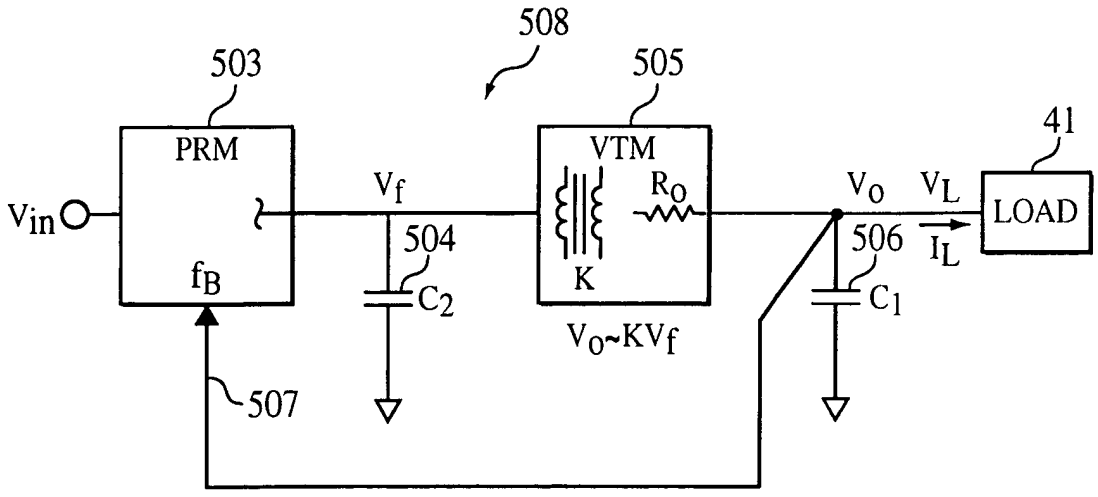

508
503
505
41
PRM
VTM
Vin
Vf
Ro
Vo
VL
LOAD
504
506
IL
fB
K
C2
C1
Vo~KVf
507

FIG. 58

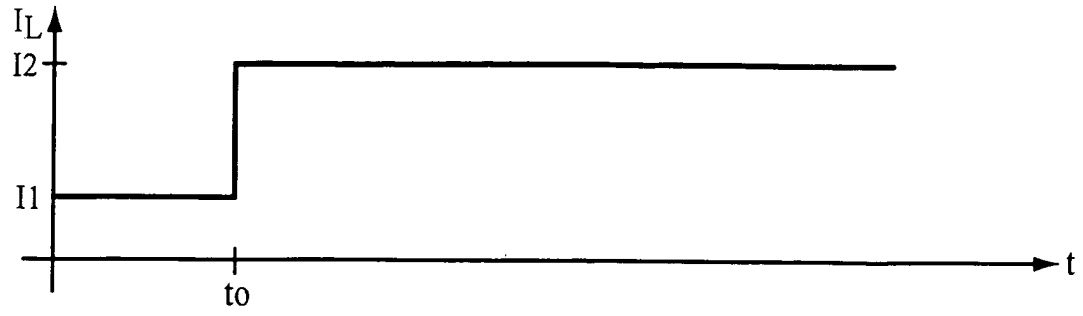


FIG. 57A

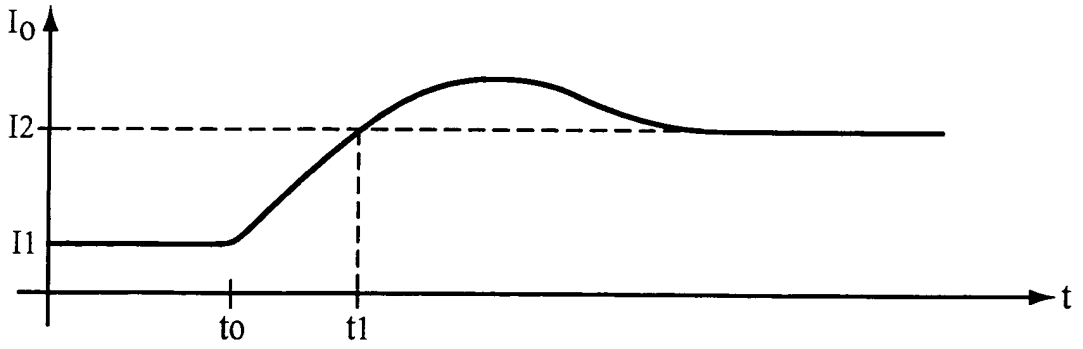


FIG. 57B

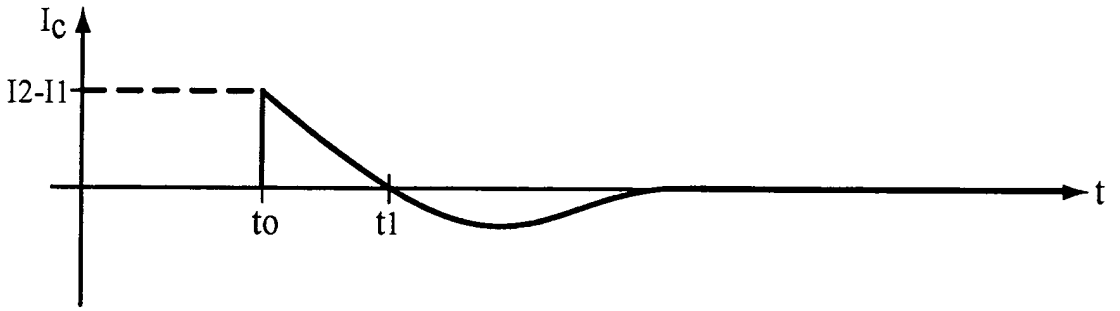


FIG. 57C

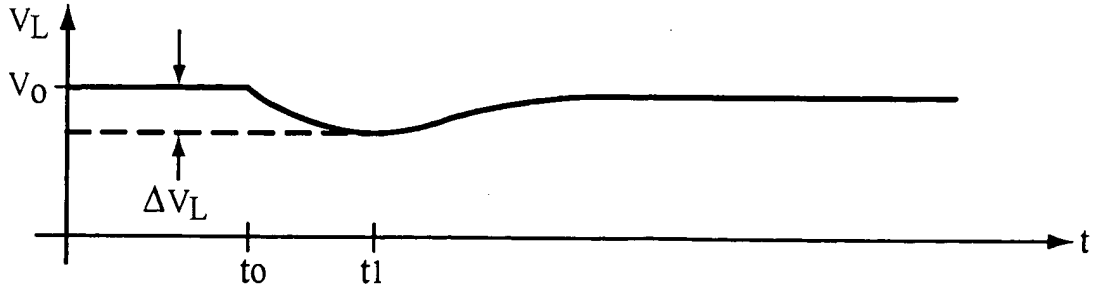


FIG. 57D

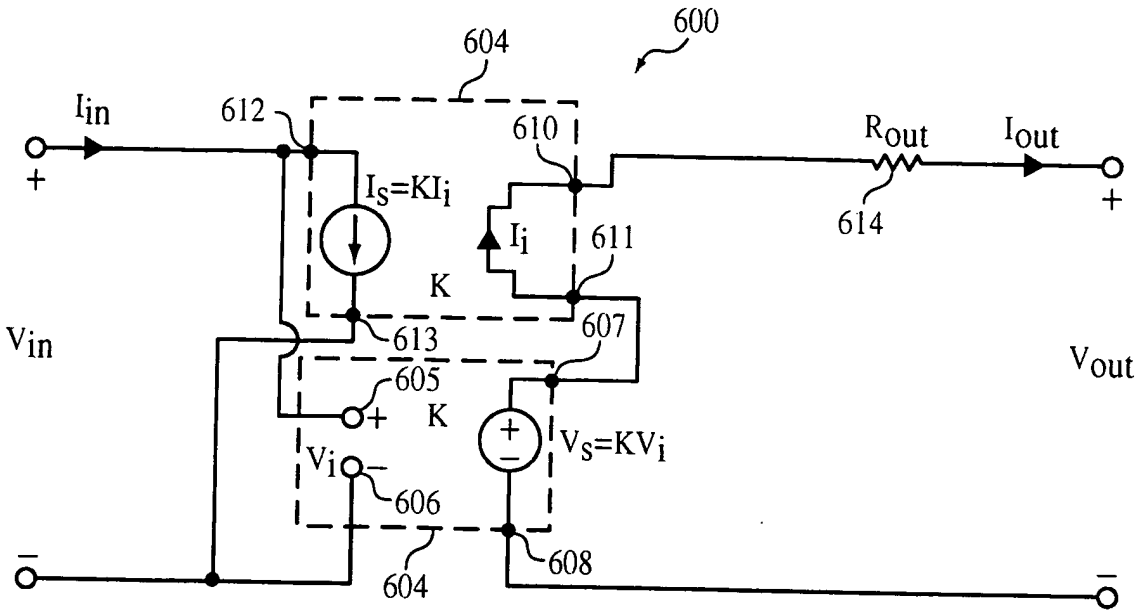


FIG. 59A

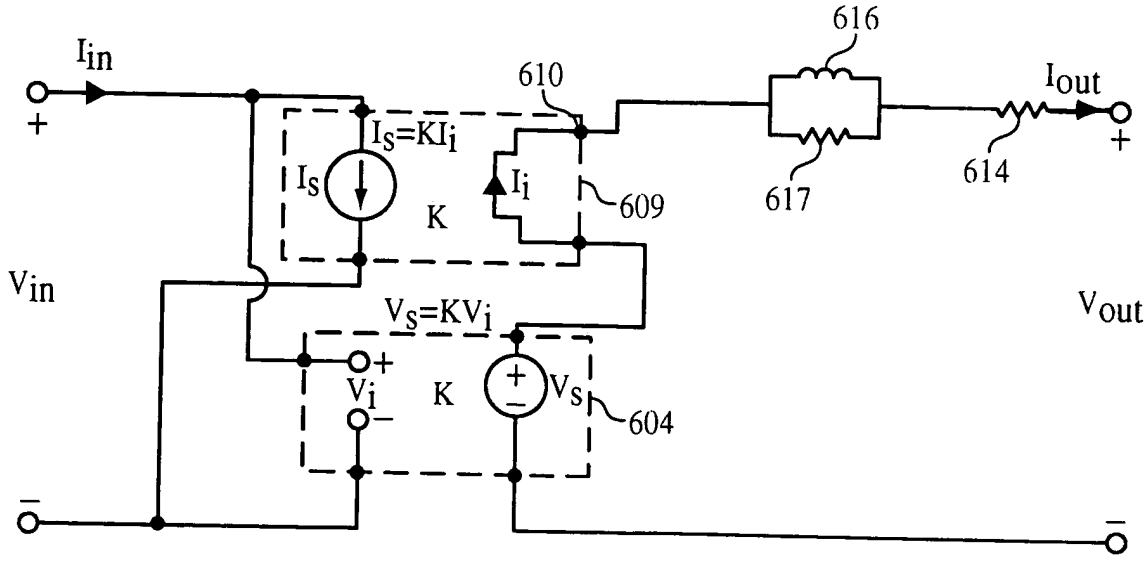


FIG. 59B

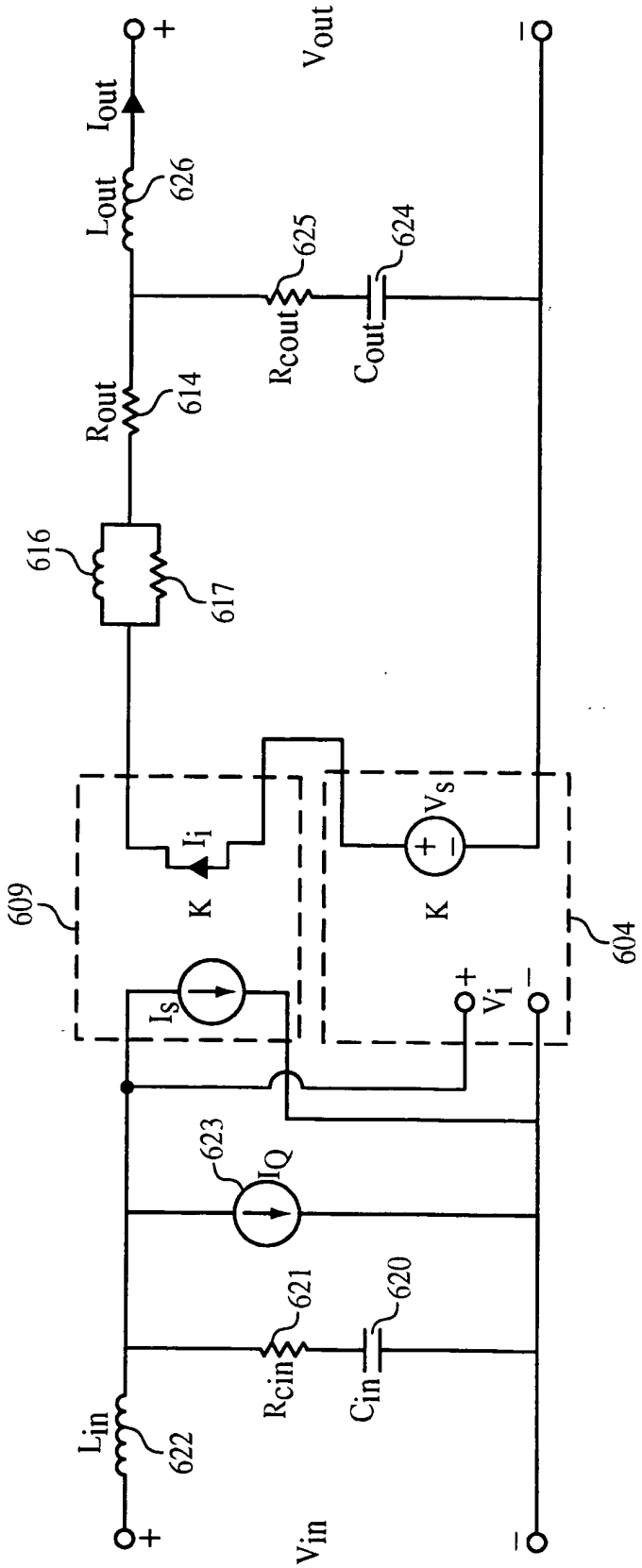

+
Vout
−
Iout
Lout
626
625
624
Rcout
Cout
Rout
614
616
617
609
Ii
K
Vs
K
604
Is
+
Vi
−
623
IQ
621
620
Rcin
Cin
Lin
622
+
Vin
−

FIG. 59C